



IEEE 2009 INTERNATIONAL SOI CONFERENCE



35th ANNUAL CONFERENCE and 15th ANNUAL SHORT COURSE

Sponsored by the Institute of Electrical and Electronics Engineers, Inc.
and Electron Devices Society

OCTOBER 5 - 8, 2009

CROWNE PLAZA HOTEL • FOSTER CITY, CALIFORNIA

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QUICK INFORMATION

HOTEL OR ROOM RESERVATION

Crowne Plaza Hotel
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TEL: 650.570.5700 • FAX: 650.570.0540
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RESERVATIONS

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CONFERENCE OR REGISTRATION

Conference Manager
BACM
578 Washington Blvd., #350
Marina del Rey, CA 90292
TEL: 310.305.7885 • FAX: 310.305.1038
bobbi@bacminc.com
www.soiconference.org
Registration via fax or mail only.

GENERAL CHAIR'S MESSAGE

On behalf of the Conference Committee, I am pleased to welcome you to the 2009 IEEE International Silicon on Insulator (SOI) Conference, the leading forum for the interaction of scientists and engineers interested in all aspects of SOI technology.

Providing a comprehensive review of the current state of the technology, the Conference will comprise a Technical Program, the principal activity; a Short Course; a Fundamentals Class; and an evening Panel Discussion. In addition, the Conference experience will be enhanced by its location and informal atmosphere as well as the social events planned for attendees and their guests.

The theme of this year's Short Course is "Ultra-thin SOI Devices: The Way to the Future." Five renowned experts in the field will provide a comprehensive overview of the operation and technology of these advanced fully depleted SOI device architectures. The topics covered include: process, process integration, electrical operation, device physics, modeling, and circuit design, including memory applications. The Short Course, organized by Dr. Jean-Luc Pelloie of ARM, will be presented Monday, October 5th.

The Technical Program Committee, chaired by Dr. Carlos Mazure of Soitec, has selected a truly exceptional set of papers that substantially advance the field. The new information will broaden the perspectives of active specialists as well as provide the necessary background for newcomers to SOI technology. The Plenary Session, which kicks off the Technical Program on Tuesday, October 6th, will feature three invited speakers discussing various timely topics of keen interest to the SOI Community.

On Wednesday afternoon, October 7th, an SOI Device and Circuit Fundamentals class is offered that will provide attendees an opportunity to improve their skills and understanding of SOI device operation and SOI circuit design. The two classes will cover the basic physics, performance comparison, and scaling limits of SOI devices and various aspects of SOI Analog circuit design in-

cluding noise, ESD, passive components, and low power design. This educational class, organized by Dr. Samuel Fung of TSMC, will be instructed by two prominent experts of the SOI community.

The topic of the Evening Panel Discussion on Wednesday evening, October 7th, is "Issues and Opportunities in Circuit Design: Bulk vs. PDSOI vs. FDSOI." The panel, organized by Dr. Bruce Doris of IBM, will be comprised of distinguished industry experts conveying and supporting their views on this important topic. We look forward to a lively debate as the audience will be encouraged to challenge panel members with alternate opinions.

Our social program will include a welcome reception the evening of October 5th; a banquet the evening of October 6th, with a presentation by Douglas C. Maclise of NASA. Mr. Maclise's talk is entitled "NASA Avionics, the path we've followed and where we're going." He will present a brief history of NASA, the role of electronics, and talk about where NASA is going next. Also, a casual networking dinner is planned for the evening of October 8th, which has been a favorite venue in the past to unwind and catch up with our colleagues from around the world.

I would like to acknowledge the hard work and dedication of the executive and technical committees, as well as the conference management team, for putting together this exceptional program, in these challenging times. More importantly, let me express my deep appreciation to the authors who submitted papers; their herculean efforts and dedication is at the core of the Conference, which provides a significant yearly contribution to the progress of SOI technology.

Sincerely,
Mario M. Pelella, General Chair

EXECUTIVE COMMITTEE

GENERAL CHAIR

Mario M. Pelella, *tau-Metrix*
mario.pelella@tau-Metrix.com

Mario M. Pelella received his BS and MS degrees in electrical engineering from Clarkson University, Potsdam, NY, in 1983 and 1985, respectively. He received his PhD degree in electrical and computer engineering at the University of Florida, Gainesville in 2000.

Dr. Pelella joined IBM Microelectronics (General Technology) Division in 1985 where he worked on the device design and modeling of advanced high-speed bipolar transistor technologies and contributed to the development of advanced Silicon-on-Insulator (SOI) CMOS technologies for IBM's, DARPA's, and NCCOSC's Low Power Electronics programs. In 1996 he joined the Silicon Technology Innovation and Modeling group at

the IBM T.J. Watson Research Center, Yorktown Heights, NY where he worked on improvements to TCAD modeling tools and the analysis of floating-body effects in scaled PD/SOI technologies. He joined the Logic Technology Development group at Advanced Micro Devices in 2000 where he worked on the development of scaled SOI technologies for the next generation of high-performance microprocessors. In 2008, he joined tau-Metrix, Inc. to help develop non-contact performance-based metrology technologies and is currently their Vice President of Engineering. His research and development interest continue to include the device design, modeling, and performance analysis of advanced CMOS (including SOI) technologies, as well as Electrostatic Discharge

(ESD) protection devices, and is an author of over 50 refereed publications.

Dr. Pelella was chairman of the IEEE Electron Device Society Mid Hudson Valley Chapter, 1995-1997, participated on the 1995-1996 and 1996-1997 National Technology Roadmap Committee for Semiconductor Compact Modeling, served on the IEEE International SOI Conference technical program committee during 1996-1998 and is now participating on the 2009 SOI Conference executive committee as the General Chair. He was the recipient of the Semiconductor Research Corporation (SRC) outstanding industrial mentor award in 1996. He received a 1983, 1984 TI Fellowship award and a 1998, 1999 IBM Cooperative Fellowship award to pursue his academic research.

TECHNICAL PROGRAM CHAIR

Carlos Mazure, *Soitec*
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Carlos Mazure, Chief Technology Officer, Executive Vice President of Soitec is involved in defining Soitec's technology strategy and leads advanced technology alliances with customers and universities, including European Union and French R&D programs. Head of R&D, he is tasked with identifying the best breed of engineered substrates and substrate technologies to help define future development directions for the com-

pany. He works closely with Soitec's Business Unit Technology Platforms, Business Development organization and customers to support existing programs and help identify new applications. He joined Soitec in 2001 to create the R&D organization.

Prior to joining Soitec, Dr. Mazure served as director of business development at Infineon Technologies AG. He worked for the IBM/Infineon DRAM Development Alliance in East Fishkill, New York. His experience also includes work on SOI, BiCMOS high performance SRAM and technology development at APRDL, Mo-

torola Semiconductor in Austin, Texas.

Mazure holds two doctorates in physics, one from the University of Grenoble, France, and the other from the Technical University of Munich, Germany. He has authored or co-authored more than 150 technical papers and holds more than 90 patents worldwide. He is a member of several international technology and advisory committees, IEEE member and a regular invited speaker at international conferences and workshops.

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EXECUTIVE COMMITTEE

continued

LOCAL ARRANGEMENTS CHAIR

Weize (Wade) Xiong,
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Weize (Wade) Xiong received his PhD in electrical engineering from University of California, Davis in 2001.

TREASURER/REGISTRATION CHAIR

Malgorzata Jurczak, IMEC
jurczakm@imec.be

Malgorzata Jurczak received her MSc and PhD degrees in electrical engineering from the Warsaw University of Technology (WUT). In 1991 she joined WUT where she worked on modeling of MOS SOI devices. In 1994 she was with NMRC, Cork, Ireland and in 1997 with Kyung Hee University, Seoul, Korea. In 1998 she

PUBLICITY & DEVELOPMENT CHAIR

Pierre Fazan,
Innovative Silicon, Inc.
pfazan@z-ram.com

Pierre C. Fazan was born in Lausanne, Switzerland where he obtained his physics diploma and PhD degrees at the Swiss Federal Institute of Technology (EPFL) in 1984 and 1988 respectively. From 1989 to 1997 he worked as process integration engineer then manager at Micron Technology, Boise, Utah, focusing on DRAM bit cell architecture and

Prior to graduate study, he was with Texas Instruments from 1995-1997 as product engineer. From 2000-2002, he led Cypress Semi-Conductor 90nm low power CMOS transistor development. He returned to TI in 2003. From 2003 to 2006 he was in charge of multi-gate transistors and nano-wire

joined CNET, France Telecom in Grenoble. She was involved in development of 0.18 and 0.12 μ m CMOS process and alternative approaches for sub-0.1 μ m CMOS (strain Si, vertical transistor, SON). In 2000 she joined IMEC, Leuven, Belgium. In the years 2000-2003 she was the IMEC coordinator of the JDP program with Philips on device process integration for 90nm and 65nm CMOS. In years 2003-2007 she was the group leader of the Device Implementation Projects in the CMOS department and the

DRAM process integration. In 1997 he was named part-time Technology Manager at EM Microelectronics, Marin, Switzerland, and part-time Professor at the Swiss Federal Institute of Technology, Lausanne, EPFL, where he is teaching in the field of IC manufacturing. From 1999 to 2001 he performed various consulting contracts for the IC industry focused on DRAM, embedded DRAM and Non Volatile Memory integration and architecture. In 2002 he co-founded Innovative Silicon Inc., developing a new Floating Body single transistor

transistors research evaluations. Wade is currently part of TI's 32nm node low power CMOS development team. Dr. Xiong has authored and co-authored over 50 journal/conference papers and a book chapter on Multi-Gate MOSFET Technologies. He is a senior member of IEEE.

project manager of IMEC Industrial Affiliated Program EMERALD on MUGFET devices. Currently she is the program manager of NVM and Emerging Memories program. She holds 17 European and American patents, and authored and co-authored more than 200 publications. In 2000 she received the Paul Rappaport Award for the best paper published in IEEE TED. She has been a member of scientific committees of IEDM, ESSDERC, VLSI TSA and IEEE SOI conferences and ITRS Roadmap.

memory technology. This company was funded by venture capitalists in 2003. Within Innovative Silicon Inc., Dr. Fazan acted first as CEO and is currently the Chairman of the Board and CTO. He has authored or co-authored more than 100 papers in the field of semiconductor devices and memory integration and invented or co-invented more than 180 US patents. Dr. Fazan has served as member in program committees of the SOI Conference, IEDM, VLSI Tech. Symp, ISIF, ESSDERC, INFOS, ICMTD and ECS Conferences.

SENIOR COMMITTEE

RUMP & POSTER CHAIR

Bruce Doris, IBM
dorisb@us.ibm.com

Bruce Doris was born and grew up in Connecticut. Throughout his time in graduate school he worked at Sematech and Advanced Products Research and Development at Motorola in the

area of materials research. In 1997 he obtained a PhD in physics at the University of Texas at Austin. From 1997 to 2000 he held various positions at IBM Microelectronics including Yield Enhancement, Process Development and Process Integration. He joined IBM Research in 2001 and worked in the area of Exploratory Devices. In 2007, Bruce and his family moved to

Albany, NY. Currently he manages the Device Integration Research department at IBM at Albany Nanotech. He has authored or co-authored over 100 papers and holds well over 100 US patents. Bruce's research interests include Extremely Scaled Transistors, Local Mechanical Stress Technology and Alternate Device Architectures.

SHORT COURSE CHAIR

Jean-Luc Pelloie,
SOISI /ARM France
jean-luc.pelloie@arm.com

Jean-Luc Pelloie co-founded SOISIC in April 2001, the first independent company offering SOI IP blocks such as libraries of standard cells, I/O cells, and memory compilers. He joined ARM at the end of 2006 as Director of SOI Technology as a result of

SOISIC's acquisition. He received his PhD degree in 1984 from the Institut National des Sciences Appliquées de Lyon. For more than ten years he managed the SOI CMOS developments at LETI (Grenoble-France) where several technology generations were developed from 1.2 μm down to 90 nm. He worked for one year at the IBM Watson Research Center to manage an IBM/LETI SOI program in 93/94 and managed a

TI/LETI program for advanced SOI CMOS. His SOI expertise covers both fully-depleted and partially-depleted transistor architectures, including process integration, electrical characterization, Spice modeling and circuit design at transistor level. He has authored and co-authored more than 100 technical papers and is regularly invited to give presentations at renowned international conferences.

FUNDAMENTALS CLASS CHAIR

Samuel Fung, TSMC
khfung@tsmc.com

Samuel K. H. Fung received his PhD in electrical engineering from the Hong Kong University of Science and Technology in 1998. His PhD thesis is on "Thin-film SOI Device Physics and Fabrication" under supervision of Prof. Ping K. Ko. From 1997-98, Samuel

was a visiting student in UC Berkeley under supervision of Prof. Chenming Hu. In 1998, Samuel joined IBM Microelectronics SRDC at Fishkill, New York. At IBM, Samuel has involved in early PD-SOI model development and 90nm SOI CMOS transistor development, which is the technology behind PS3/XBOX-360/Wii game consoles. In 2002, Samuel joined TSMC. In TSMC, Samuel has made contribution in the transistor development of

65nm, 40nm and currently 22nm node. Together with Chenming Hu and Pin Su, Samuel has developed the BSIM family of SOI model for FD/PD simulation. In 2001, BSIMPD was selected as the industry standard compact model for PD-SOI technology. Samuel has 10 patents filed and has authored or co-authored over 60 research papers.

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SENIOR COMMITTEE continued

MULTIMEDIA CHAIR

Vyshnavi Suntharalingam,
MIT Lincoln Lab
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Vyshnavi Suntharalingam received her B.S. in electrical engineering from Yale University in 1989 and her Ph.D. from Penn State University in 1996 with a specialization in the design,

simulation, fabrication, and characterization of thin film solar cells and transistors. She has been a member of the Advanced Silicon Technology Group at Lincoln Laboratory since 1996, serving as Assistant Group Leader for 4.5 years. She developed process technology and device designs to integrate low voltage CCD image sensors with SOI-CMOS cir-

cuitry for low-light level applications. Since 2005 she is a Senior Member of the Technical Staff, and leads projects to design, fabricate, package, and characterize 3-D integrated CMOS image sensors. Her principal interests are in SOI-CMOS and CCD device design, fabrication, and characterization, particularly for low-power, scientific focal planes.

TECHNICAL COMMITTEE

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CONFERENCE AT-A-GLANCE

MONDAY, October 5th

- 7:00am **Short Course Breakfast** (optional course)
- 8:00am Short Course
- 11:30am Short Course Lunch
- 12:45pm Short Course
- 6:00pm **Welcome Reception**

TUESDAY, October 6th

- 7:00am **Continental Breakfast**
- 8:00am Introduction & Welcome
- 8:15am Session 1: PLENARY SESSION
- 10:15pm **Break**
- 10:30am Session 2: NOVEL LAYER TRANSFER APPLICATIONS
- 12:50pm **Lunch (on own)**
- 1:50pm Session 3: SRAM, 1T DRAM, & IMAGERS
- 4:30pm Session 4: POSTER SESSION
- 7:00pm **Banquet**

WEDNESDAY, October 7th

- 7:00am **Continental Breakfast**
- 8:00am Session 5: SOI DESIGN
- 10:00am **Break**
- 10:15am Session 6: SOI APPLICATIONS
- 11:45am **Break**
- 12:00pm Session 7: 3D TECHNOLOGY
- 1:10pm **Lunch & Free time**
- 2:15pm Fundamentals Class: "SOI Device and Circuit Fundamentals" (optional)
- 6:30pm **Networking Dinner**
- 8:00pm Evening Panel Discussion:
"Issues and Opportunities in Circuit Design Bulk vs PDSOI vs FDSOI"

THURSDAY, October 8th

- 7:00am **Continental Breakfast**
- 8:00am Session 8: FDSOI TECHNOLOGY
- 10:00am **Break**
- 10:20am Session 9: SUBSTRATE TECHNOLOGY
- 12:40pm **Lunch (on own)**
- 1:40pm Session 10: NANOWIRES & ADVANCED DEVICES
- 3:15pm **Break**
- 3:30pm Session 11: LATE NEWS
- 4:50pm Wrap-up & Presentation of Best Paper & Best Student Paper Awards

TECHNICAL SESSIONS

THE TECHNICAL PROGRAM will consist of 30 oral and 13 poster papers, as well as 16 invited talks. Technical Sessions and Session Chairs are as follows:

- | | | | |
|------------------|---|-------------------|--|
| SESSION 1 | PLENARY
Carlos Mazure, Mario Pelella | SESSION 7 | 3D Technology
Malgorzata Jurczak,
Vyshnavi Suntharalingam |
| SESSION 2 | Novel Layer Transfer Applications
Juthika Basak, Jerry Zimmer | SESSION 8 | FDSOI Technology
Bruce Doris, Bich-Yen Nguyen |
| SESSION 3 | SRAM, 1T DRAM, & Imagers
Wade Xiong, Uygur Avci | SESSION 9 | Substrate Technology
Samuel Fung, Maud Vinet |
| SESSION 4 | Posters
Bruce Doris | SESSION 10 | Nanowires & Advanced Devices
Les Palkuti, Toshiro Hiramoto |
| SESSION 5 | SOI Design
Jean-Luc Pelloie, Pierre Fazan | SESSION 11 | LATE NEWS
Mario Pelella, Carlos Mazure |
| SESSION 6 | SOI Applications
Frederic Giancesello, Jiro Ida | | |

TECHNICAL PROGRAM SCHEDULE

- | | |
|------------------|---|
| SESSION 1 | PLENARY |
| 8:15am | 1.1 FDSOI for Low Power CMOS , Ghavam Shahidi • IBM (invited) |
| 8:55am | 1.2 Review of FinFET Development , Malgorzata Jurczak • IMEC (invited) |
| 9:35am | 1.3 SOI Design , Rich Goldman • Synopsys (invited) |
| SESSION 2 | Novel Layer Transfer Applications |
| 10:30am | 2.1 Si on Glass , George Wildemann, Corning (invited) |
| 10:50am | 2.2 Submicron Single Crystal Si TFTs on a Large Glass Substrate
Y. Takafuji, Y. Fukushima, K. Tomiyasu, M. Takei, M. Moriguchi, Y. Ogawa, T. Itoga, H. Kobayashi,
¹ Y. Watanabe, ¹ E. Kobayashi, ² S. R. Droes, ² A.T. Voutsas, ² J. Hartzell • Display Device Labs, Corporate
R&D Group, Sharp Corporation; ¹ Electronic Component Group, Sharp Corporation; ² Sharp Labora-
tories of America, Inc. |
| 11:10am | 2.3 Demonstration of Low Temperature CMOS Devices on SiOG and SOI Substrates
C. Kosik Williams ¹ , J.G. Couillard ¹ , J. Senawiratne ¹ , R.G. Manley ² , P.M. Meller ² , C.G. Shea ² ,
A.M. McCabe ² , K.D. Hirschman ² • ¹ Corning Incorporated; ² Microelectronic Engineering Dept.,
Rochester Institute of Technology |

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TECHNICAL PROGRAM SCHEDULE continued

- 11:30am 2.4 **From Silicon Direct Wafer Bonding to Surface Nano-Patterning: a way to innovative substrate elaboration**
F. Fournel, A. Bavard, J. Eymery¹ • CEA, LETI, MINATEC; ¹CEA/INAC (invited)
- 11:50am 2.5 **High-Efficiency Solar Cell Embedded in SOI Substrate for ULP Autonomous Circuits**
O. Bulteel, R. Delamare, D. Flandre • Microelectronics Lab., Université catholique de Louvain
- 12:10am 2.6 **Thermal Actuation of High Frequency Micromechanical Resonators**
A. Rahafrouz, A. Hajjam, S. Pourkamali • Department of Electrical and Computer Engineering, University of Denver
- 12:30pm 2.7 **Smart Stacking Technology, Bernard Aspar • Soitec (invited)**

SESSION 3 SRAM, 1T DRAM, & Imagers

- 1:50pm 3.1 **SRAM Improvements with FDSOI Technology, Tsu Jae King • UC Berkeley (invited)**
- 2:10pm 3.2 **Investigation of Static Noise Margin of FinFET SRAM Cells in Sub-threshold Region**
M.-L. Fan, Y.-S. Wu, V. P.-H. Hu, P. Su, C.-T. Chuang • Department of Electronics Engineering, National Chiao Tung University
- 2:30pm 3.3 **Analyze of Temporal and Random Variability of a 45nm SOI SRAM Cell**
Y. Laplanche • ARM
- 2:50pm 3.4 **Impact of FinFET Technology on 6T-SRAM Performance**
S. O'uchi, T. Nakagawa, T. Matsukawa, Y.X. Liu, K. Endo, T. Sekigawa, K. Sakamoto, H. Koike M. Masahara • Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST)
- 3:10pm 3.5 **SRAM Yield Enhancement with Thin-BOX FD-SOI**
¹C. Shin, ¹M. H. Cho, ²Y. Tsukamoto, ¹T.-J. K. Liu • ¹Department of Electrical Engineering and Computer Sciences, University of California, Berkeley; ²Renesas Technology Corp
- 3:30pm 3.6 **Analysis of sense margin and reliability of 1T-DRAM fabricated on thin-film UTBOX substrates**
N. Collaert, M. Aoulaiche, M. Rakowski, B. De Wachter, K. Bourdelle¹, B.-Y. Nguyen², F. Boedt¹, D. Delprat¹, M. Jurczak • IMEC; ¹SOITEC; ²SOITEC-USA
- 3:50pm 3.7 **Effect of Source/Drain Asymmetry on the Performance of Z-RAM® Devices**
N. R. Mohapatra, R. vanBentum, E. Pruefer, W. P. Maszara, C. Caillat¹, Z. Chalupa¹, Z. Johnson¹, D. Fisch¹ • AMD Fab36 LLC & Co. KG; ¹Innovative Silicon
- 4:10pm 3.8 **SOI Applications in China, Ming Chen • Simgui (invited)**

TECHNICAL PROGRAM SCHEDULE continued

SESSION 4 Posters

- 4:30pm 4.01 **Design and Fabrication of SOI-Based MEMS for Mechanical Memory Storage**
A. Parent, C.-M. Tasseti, J. Haussy, A. Tissot • CEA, DAM, DIF
- 4.02 **Engineering Silicon-On-Insulator (SOI) Substrates for Hybrid Orientation Technologies (HOT)**
T. Signamarcheix¹, B. Biasse¹, A.-M. Papon¹, E. Nolot¹, B. Ghyselen², L. Clavelier¹ • ¹CEA, LETI; ²SOITEC
- 4.03 **Thermal Sensing Performance of Lateral SOI PIN Diodes in the 90 – 400 K Range**
M. de Souza¹, B. Rue², D. Flandre², M. A. Pavanello¹ • ¹Centro Universitário da FEI; ²Université catholique de Louvain
- 4.04 **LDD Depletion Effects in Thin-BOX FDSOI Devices with a Ground Plane**
R. Yan¹, R. Duane¹, P. Razavi¹, A. Afzalilian¹, I. Ferain¹, C.W. Lee¹, N. Dehdashti-Akhavan¹, K. Bourdelle², B.Y. Nguyen³, J.P. Colinge¹ • ¹Tyndall National Institute; ²SOITEC; ³SOITEC-USA
- 4.05 **Fabrication of Compressively-Strained GeOI Substrates using the Smart Cut(tm) Technology**
E. Augendre, L. Sanchez, J.-M. Hartmann, W. Van Den Daele¹, S. Favier, E. Guiot², B. Ghyselen², K. K. Bourdelle², S. Cristoloveanu¹, T. Billon, L. Clavelier • CEA, LETI, Minatec; ¹IMEP-INP Grenoble-Minatec; ²SOITEC
- 4.06 **LD MOS transistors on Si-on-SiC hybrid substrates having crystalline or poly-crystalline SiC - Electrical and thermal characterization**
Ö. Vallin, L.-G. Li, H. Norström, U. Smith, J. Olsson • Uppsala University, The Ångström Laboratory, Solid State Electronics
- 4.07 **Transconductance Ramp Effect in High-k Triple Gate sSOI nFinFETs**
J. A. Martino¹, P. G. D. Agopian¹, N. Collaert², E. Simoen², C. Claeys^{2,3} • ¹LSI/PSI/USP, University of Sao Paulo; ²IMEC; ³E.E. Dept., KU Leuven
- 4.08 **Germanium MOS Transistors on sapphire and alumina platforms**
P. T. Baine, H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, D. W. McNeill, P. V. Rainey, Y. H. Low, Y. W. Low, D. Tantraviwat • Northern Ireland Semiconductor Research Centre, School of Electronics, Electrical Engineering & Computer Science, Queen's University, Belfast
- 4.09 **Novel Architecture for Inertial Grade SOI MEMS Inertial Sensors**
A. A. Aziz¹, A.-H. Sharaf^{1,2}, S. Sedky^{1,3} • ¹Science and Technology Research Center (STRC), American University in Cairo (AUC); ²National Center for Radiation Research and Technology (NCRRT), Egyptian Atomic Energy Authority (EAEA); ³Physics Department, AUC
- 4.10 **Effect of Substrate Rotation on the Analog Performance of Triple-Gate FinFETs**
M. A. Pavanello^{1,2}, J. A. Martino², E. Simoen³, N. Collaert³, C. Claeys^{3,4} • ¹Centro Universitário da FEI; ²LSI/PSI/USP, University of Sao Paulo; ³IMEC; ⁴E.E. Dept., KU Leuven

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TECHNICAL PROGRAM SCHEDULE continued

- 4.11 **A New Technique for Localized Formation of SOI Active Regions**
B. Veeramachaneni¹, J. Winans², P.M. Fauchet², K. Witt³, K.D. Hirschman¹ • ¹Department of Microelectronic Engineering, Rochester Institute of Technology; ²Department of Electrical and Computer Engineering, University of Rochester; ³Semiteol, Inc.
- 4.12 **An Internally Amplified Signal SOI Nano-bridge Biosensor for Electrical Detection of DNA Hybridization**
K.B. Parizi, N. Melosh, Y. Nishi • Electrical Engineering Department, Stanford University
- 4.13 **Quantum Confinement Effect in Short-Channel Gate-All-Around MOSFETs and Its Impact on the Sensitivity of Threshold Voltage to Process Variations**
Y.-S. Wu, P. Su • Department of Electronics Engineering, National Chiao Tung University

SESSION 5 SOI Design

- 8am 5.1 **SOI Design for High Performance**, *Ken Chang* • Rambus (invited)
- 8:30am 5.2 **SOI Design Libraries**, *Christophe Frey* • ARM (invited)
- 9:00am 5.3 **Ultra-Low-Power High-Noise-Margin Logic with Undoped FD SOI Devices**
D. Bol, J. De Vos, D. Flandre, J.-D. Legat • Université catholique de Louvain
- 9:20am 5.4 **Multiple Independent Gate FET Ring Oscillators with Dynamic Frequency Tuning**
D.G. Wilson, B.N. Meek, K.J. DeGregorio, D.R. Hackler • American Semiconductor, Inc.
- 9:40am 5.5 **Enhanced performance of SERDES current-mode output driver using 0.13 μ m PD SOI CMOS**
D. Kamel¹, M. Dessouky², D. Flandre¹ • ¹Microelectronics Laboratory (DICE), Université catholique de Louvain; ²Faculty of Engineering, Ain Shams University

SESSION 6 SOI Applications

- 10:15am 6.1 **Silicon-on-Sapphire, a Replacement for Gallium Arsenide?**
George. P. Imthurn • Peregrine (invited)
- 10:45am 6.2 **Channel Engineering of SOI MOSFETs for RF Applications**
C.L. Chen, J.M. Knecht, J. Kedzierski, C.K. Chen, P.M. Gouker, D-R. Yost, P. Healey, P.W. Wyatt, C.L. Keast • Lincoln Laboratory, Massachusetts Institute of Technology
- 11:05am 6.3 **DC and RF Temperature Behavior of Deep Submicron Graded Channel MOSFETs**
M. Emam¹, A. Kumar², J. Ida², F. Danneville³, D. Vanhoenacker-Janvier¹, J.-P. Raskin¹ • ¹EMIC, Microwave Laboratory - Université catholique de Louvain; ²Semiconductor R&D Department, OKI Semiconductor Co. Ltd.; ³Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN)
- 11:25am 6.4 **45 GHz Silicon MESFETs on a 0.15 μ m SOI CMOS Process**
W. Lepkowski, S.J. Wilk, T.J. Thornton • Arizona State University

TECHNICAL PROGRAM SCHEDULE continued

SESSION 7 3D Technology

- 12:00pm 7.1 3D Systems, Subramanian Iyer • IBM (invited)
- 12:30pm 7.2 **Radiation Effects in MIT Lincoln Laboratory's 3DIC Technology**
P.M. Gouker, P.W. Wyatt, D-R. Yost, C.K. Chen, J.M. Knecht, C.L. Chen, and C.L. Keast • Lincoln Laboratory, Massachusetts Institute of Technology
- 12:50pm 7.3 **Results on Aligned SiO₂/SiO₂ Direct Wafer-to-Wafer Low Temperature Bonding for 3D Integration**
A. Garnier¹, M. Angermayer², L. Di Cioccio¹, P. Gueguen¹, T. Wagenleitner² • ¹CEA Leti; ²EV Group

SESSION 8 FDSOI Technology

- 8:00am 8.1 **FD-SOI MOSFETs for the Low-Voltage Nanoscale CMOS Era**
K. Itoh, N. Sugii, D. Hisamoto, R. Tsuchiya • Hitachi (invited)
- 8:20am 8.2 **Comparison of Ultra-Low-Power and static CMOS full adders in 0.15 Cm FD SOI CMOS**
D. Kamel, D. Bol, F-X. Standaert, D. Flandre • Microelectronics Laboratory (DICE), Universite catholique de Louvain,
- 8:40am 8.3 **Platinum Silicide Metallic Source and Drain Process Optimization for FDSOI pMOSFETs**
V. Carron¹, F. Nemouchi¹, Y. Morand², T. Poiroux¹, M. Vinet¹, S. Bernasconi², O. Louveau², D. Lafond¹, V. Delaye¹, F. Allain¹, S. Minoret¹, L. Vandroux¹, T. Billon¹ • ¹CEA-LETI/Minatec; ²STMicroelectronics
- 9:00am 8.4 **Expanding Opportunities of Ultra Low Power and Harsh Applications with Fully Depleted (FD) SOI**
J. Ida^{1,2}, K. Tani², M. Ohono², M. Yanagihara², Y. Igarashi², K. Sakamoto² • ¹Department of Electrical and Electronic Engineering, College of Engineering, Kanazawa Institute of Technology; ²Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST) (invited)
- 9:20am 8.5 **Modeling of Electron Tunneling in SOI-MOSFET and Its Influence on Device Characteristics**
T. Hayashi¹, N. Sadachika¹, T. Murakami¹, D. Sugiyama¹, S. Yukuta¹, S. Kusu¹, K. Johguchi¹, M. Miyake¹, H. J. Mattausch¹, M. Miura-Mattausch^{1,2}, S. Baba, J. Ida² • ¹Hiroshima University; ²Oki Semiconductor Co.
- 9:40am 8.6 **New method to extract interface states density at the Back and the Front gate interfaces of FDSOI transistors from CV-GV measurements**
L. Brunet^{1,2,3}, X. Garros², F. Andrieu², G. Reibold², E. Vincent¹, A. Bravaix³, F. Boulanger² • ¹STMicroelectronics; ²CEA-Leti/Minatec; ³IM2NP,

SESSION 9 Substrate Technology

- 10:20am 9.1 **Ultra thin SOI for FDSOI Technology**, Daniel Delpra • Soitec (invited)
- 10:50am 9.2 **Silicon-on-Glass (SiOG) Substrate Technology: Process and Materials Properties**
J. S. Cites, J. G. Couillard, K. P. Gadkaree • Corning Incorporated

TECHNICAL PROGRAM SCHEDULE continued

- 11:10am 9.3 **Thermal Considerations for Advanced SOI Substrates Designed for III-V/Si Heterointegration**
N. Yang¹, M. T. Bulsara¹, E. A. Fitzgerald¹, W.K. Liu², D. Lubyshev², J.M. Fastenau², Y. Wu², M. Urtega³, W. Ha³, J. Bergman³, B. Brar³, C. Drazek⁴, N. Daval⁴, F. Letertre⁴, W.E. Hoke⁵, J.R. LaRoche⁵, K.J. Herrick⁵, T.E. Kazior⁵ • ¹Materials Science and Engineering, MIT; ²IQE Inc.; ³Teledyne Scientific; ⁴SOITEC; ⁵Raytheon RF Components
- 11:30am 9.4 **Investigation of Ion Implantation Induced Electrically Active Defects in p-Type Silicon**
J. Senawiratne¹, J. S. Cites¹, J. G. Couillard¹, J. Moll¹, C. A. Kosik Williams¹, P. G. Whiting² • ¹Corning Incorporated; ²Microelectronic Engineering Dept., Rochester Institute of Technology
- 11:50am 9.5 **PD-SOI MOSFETs: interface effect on point defects and doping profiles**
E.M. Bazizi^{1,2,3}, A. Pakfar¹, P. F. Fazzini², F. Cristiano², C. Tavernier¹, A. Claverie³, A. Burenkov⁴, P. Pichler⁴ • ¹STMicroelectronics; ²LAAS/CNRS, University of Toulouse; ³CEMES/CNRS; ⁴Fraunhofer Institute of Integrated Systems and Device Technology (IISB)

SESSION 10 **Nanowires and Advanced Devices**

- 1:25pm 10.1 **Advanced Nano Devices**, Jason Woo • UCLA (invited)
- 1:55pm 10.2 **Optimal Design and Performance Assessment of Extremely-Scaled Si Nanowire FET on Insulator**
C.-Y. Chen¹, Y.-B. Liao², M.-H. Chiang¹, K. Kim³, W.-C. Hsu², S.-Y. Cheng¹ • ¹Department of Electronic Engineering, National Ilan University; ²Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University; ³IBM T. J. Watson Research Center
- 2:15pm 10.3 **Investigation of bias-dependent series resistances and barrier height in Double Gate Schottky MOSFETs**
J. Bhandari^{1,2}, M. Vinet¹, T. Poiroux¹, J. M. Sallese², B. Previtali¹, S. Deleonibus¹, A.M. Ionescu² • ¹CEA-LETI/Minattec; ²NanoLab, Ecole Polytechnique Fédérale de Lausanne
- 2:30pm 10.4 **Variable-Barrier Tunneling SOI Transistor (VBT)**
A. Afzalian, N. Dehdashti, I. Ferain, C.W. Lee, R. Yan, P. Razavi, J.P. Colinge • Tyndall National Institute, University College Cork
- 2:55pm 10.5 **High Temperature Performance of OTA with Non-Ideal Double Gate SOI MOSFETs**
A. Kranti, G. A. Armstrong • Semiconductor and Nanotechnology Group, School of Electronics Electrical Engineering and Computer Science, Queen's University Belfast

SHORT COURSE OVERVIEW

The conference is pleased to offer as an optional course the 35th annual Short Course, "ULTRA-THIN SOI DEVICES: THE WAY TO THE FUTURE."

32nm CMOS processes are ramping up and 22nm are under development. A conventional bulk CMOS scheme is still pursued but due to the physical limitations inherent to device scaling there is now a strong interest in alternative solutions that would enable to maintain the performance without increasing the leakage. The main difficulty is to control the short channel

effects and most of the candidates to achieve this are ultra-thin SOI devices either as 2D or 3D structures: multi-gate (MG), FinFET and more fancy names. All these devices have a common point: they are operating in a fully-depleted mode. Five renowned instructors will give an overview of these different devices dealing with related topics such as process,

process integration, electrical operation, device physics, modeling and circuit design including memories. The instructors have been selected to bring their different views on these new devices so that the audience may understand that there are several possible candidates that could lead to a potential interesting competition.

SHORT COURSE INSTRUCTORS

ANDRES BRYANT - BSEE '82 U. of Maine, PhD '86 Stanford U. Undergraduate research led to the development of ppb micro-acoustic-wave gas detectors. Graduate research led to the development of real-time scan-

ning tunneling microscopes. Joined IBM in 1986 to work on advanced device development for DRAM and Logic CMOS technologies. This work included the development and manufacturing installation of IBM's first

high-performance SOI technology. More recently, work has focused on the development of FinFET, Trigate and ETSOI devices. Has authored over 30 publications and over 40 patents.

THOMAS ERNST received his PhD degree from the National Polytechnics Institute of Grenoble, France, in 2000. From 1997 to 2000, he developed advanced SOI CMOS electrical characterization, simulation and modeling methods at STMicroelectronics with IMEP laboratory. He then joined CEA-LETI to develop novel strained-

channel CMOS architectures for 32 nm technology. In particular, he was leading strained SOI, strained Germanium, and SiGeOI CMOS integration at Leti. Since 2005, he is leading the 3D multi-channels and nanowire CMOS devices developments. His expertise is in the area of novel CMOS devices fabrication technology and

MOSFETs analytical modeling for electrical characterization. Dr. Ernst is author or co-author of over 110 technical journal papers and communications at international conferences on CMOS devices integration, modeling and characterization. He is author or co-author of more than 13 patents.

SHORT COURSE INSTRUCTORS continued

JERRY G. FOSSUM was born in Phoenix, Arizona. He received his B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Arizona, Tucson. During his graduate program he was a NASA Predoctoral Trainee. In 1971 he joined the technical staff of Sandia Laboratories, Albuquerque, NM, where he was engaged in various semiconductor device design and modeling activities, including the development of silicon solar cells. In 1978 he moved to the University of Florida, Gainesville, where he is now a Distinguished Professor of Electrical and Computer En-

gineering. His general area of expertise is semiconductor device theory, modeling, and design; his current research concerns physical, process-based device modeling for IC simulation and technology CAD, with emphasis on nonclassical SOI and multi-gate CMOS. He is the author or coauthor of approximately 300 papers published in technical journals and conference proceedings, and he has directed the research of 35 Ph.D. students. Dr. Fossum is a member of the Honorary Editorial Advisory Board of Solid-State Electronics. He was an Associate Editor for the IEEE Transac-

tions on Computer-Aided Design, and has been a Guest Editor for the IEEE Transactions on Electron Devices. He was elected a Fellow of the IEEE for "contributions to the theory and technology of silicon solar cells and transistors." He was a recipient of the Best Paper Award at the IEEE International SOI Conference, and has served on the Executive Committee of that conference. In 2004 he won the IEEE/EDS J. J. Ebers Award for "outstanding contributions to the advancement of SOI CMOS devices and circuits through modeling."

OLIVIER THOMAS received the Electronic Engineering Diploma from ISEN in 2001 and the PhD degree in microelectronics from the ENST of Paris in 2004. In 2005, he joined the CEA-LETI Laboratory in the Center for Innovation in Micro & Nanotechnol-

ogy (MINATEC), Grenoble, France. He was first involved in the development of low-power and low-leakage design solutions for digital mobile applications in 65nm Partially-Depleted SOI technology. Since 2006, he has been in charge of low power SRAM and

digital design projects in Thin Film SOI technologies. He is author or coauthor of 21 articles in international refereed journals and conferences and 13 patents.

ATSUSHI YAGISHITA received his BE degree, ME degree, and PhD in electrical engineering from the Keio University in 1987, 1989 and 2006, respectively. He joined ULSI research & development center at the Toshiba Corporation in 1989, where he worked on 64-256 megabit DRAM technology and Damascene/Replacement metal gate transistor technology. From 2001 to 2003, he was a

visiting researcher at the University of California, Berkeley. His research topic there was Schottky source/drain transistor with strained-Si channel technology. After returning to Toshiba Corporation, he contributed in the development of FinFET technology. From 2006, he has been with IBM-TOSHIBA System LSI Development Alliance, and was working on FinFET SRAM development at IBM TJ

Watson Research Center for two years, and his current job is Silicon-on-nothing (SON) device development at Albany Nanotechnology Center. Dr. Yagishita is a member of the IEEE Electron Device Society and the Japan Society of Applied Physics.

SHORT COURSE SCHEDULE

Monday, October 5th

7am	5pm	Registration & Information
7am	8am	Continental Breakfast
8am	8:15am	Introduction , <i>Jean-Luc Pelloie, ARM</i>
8:15am	9:45am	Multiple Gate Devices and Technology , <i>Thomas Ernst, LETI</i> <ul style="list-style-type: none">• Multiple gate devices - Motivation, families and applications (CMOS/memories), transport properties, and results from device level to circuits.• Multiple gate technologies - Some technological constraints; access resistances optimisations; 3D devices versus planar.
9:45am	10am	Break
10am	11:30am	Process & Device Technologies for FinFET and Its Alternative Devices , <i>Atsushi Yagishita, Toshiba America Electronic Components, Inc.</i> <ul style="list-style-type: none">• Introduction - FinFET vs. planar ultra-thin SOI FET• FinFET - Basic device structure; basic process flow; process; metal gate/high-k, Spacer, Source/drain; (doping, epi, silicide), Stress booster, Channel crystal orientation - Substrate comparison (SOI vs. Bulk); Hybrid of FinFET and planar FET vs. whole FinFET LSI; Process cost; Electrical characteristics• Alternative devices - FinFET family (Tri-gate, Omega-gate, Multi-gate FET, etc.); Silicon nanowire FET; Silicon on Nothing device• Conclusion and future perspective
11:30am	12:45pm	Hosted Lunch
12:45pm	2:15pm	FinFETs: The Answer to the End of Scaling? , <i>Andres Bryant, IBM</i> <ul style="list-style-type: none">• Why is the allure of thin-body double-gated FETs SCE control so strong?• The FinFET promise of scalable SCE - SCE theory and experiment: PDSOI/Bulk FETs vs Single-Gate Thin-Body FETs vs Double-Gate Thin-Body FETs• FinFETs performance challenges - 3D vs 2D parasitic capacitances; Current Drive• Scaled FinFET performance trends
2:15pm	2:30pm	Break
2:30pm	4pm	Multi-Gate MOSFET Physics and Design Insights , <i>Jerry Fossum, University of Florida</i> <ul style="list-style-type: none">• Introduction - MG MOSFETs, with number of gates from 1 to ∞; most probable nanoscale-CMOS ($L_g < 30\text{nm}$) MG devices.• Planar SG FD/SOI MOSFETs (with 2 gates, counting the substrate) - Basic electrostatics (1-D Poisson in UTB), gate-gate coupling; $V_t(V_{\text{sub}})$ with bulk inversion and accumulation; short-channel effects, t_{Si} vs. L_g for scalability (2-D Poisson in UTB); thin-BOX benefits, or tradeoffs; scaling limits.• Quasi-planar SOI FinFETs (with two or three gates) - Unique underlying physics, UFDG, and pragmatic design; DG vs. TG; Bulk inversion, and gate capacitance/ drive current; carrier mobilities (without strain); quasi-ballistic and ballistic transport; G-S/D underlap; V_t adjustment via limited S/D dopants in channel; scalability, and projected performance vs. bulk-Si MOSFETs• Floating-body DRAM Cells - Operation, issues and 1T vs. 2T.
4pm	4:15pm	Break
4:15pm	5:30pm	Advanced Circuit Design In Emerging 2D & 3D SOI Technologies , <i>Olivier Thomas, CEA-LETI</i> <ul style="list-style-type: none">• CMOS scaling and limitations• Emerging SOI device architectures• Advanced circuit design• Summary
5:30pm	5:45pm	Short Course Wrap-up , <i>Jean-Luc Pelloie, ARM</i>
6pm	7:30pm	Welcome Reception

“SOI Device & Circuits” SOI FUNDAMENTALS CLASS OVERVIEW

The SOI fundamental class is dedicated to attendees who want to get a basic knowledge of SOI MOSFET device physics and circuits design. Two lectures of 1.5 hours each will be given by world recognized experts in their respective fields, Professor Yuan Taur (University of California, San Diego) and Dr. Andrew Marshall (Texas Instruments).

Professor Taur will cover the device fundamentals of SOI MOSFETs. For any given technology node, CMOS performance is limited by the shortest channel length that can be made while maintaining robust 2-D electrostatic integrity. The scale length theories for both partially depleted and fully-depleted SOI MOSFETs will be discussed in detail,

leading to the guideline of minimum channel length as a function of the film thickness, with an emphasis on the important role of the backgate in scaling. A two-region scale length model that takes both the vertical and the lateral fields into account is needed to deal with relatively thick, high- gate dielectrics. The course will give useful guidelines that, with quantum mechanical considerations, allow the projection of scaling limits for bulk, SOI, double-gate, and nanowire MOSFETs.

Dr. Marshall will speak on Circuit Design with SOI. In some ways, circuit design in silicon-on-insulator processes varies significantly from that of conventional bulk silicon. In other aspects it can be very similar.

This class will discuss the similarities and different aspects of circuit design for partially and fully depleted silicon on insulator technologies with planar and FinFET device types.

Following a brief overview of SOI Components and Device Properties, a comparison of SOI and Bulk advantages and disadvantages will be described as a way of selecting a process for a particular application. Discussion at this point covers MOS devices, Bipolar Transistors, Diodes and Passive Components. Logic, Memory and Analog Circuit Design in SOI are discussed, together with discussion of low power design and reliability issues.

SOI FUNDAMENTALS CLASS INSTRUCTORS

ANDREW MARSHALL is a Distinguished Member of Technical Staff at Texas Instruments, in the Technology Development organization. He provides analog, digital and RF support for advanced processes, including partially depleted SOI and FinFET fully depleted SOI.

YUAN TAUR received his PhD degree in physics from University of California, Berkeley. From 1981 to 2001, he was a Research Staff Member with IBM Thomas J. Watson Research Center, Yorktown Heights, New York. Since October 2001, he is professor in the Department of Electrical and Computer Engineering, University of California, San Diego. Dr. Taur is elected a Fellow

of the IEEE in 1998. He is currently the Editor-in-Chief of IEEE Electron Device Letters, and Program Chairman of 2002 Symposium on VLSI Technology. Dr. Taur's current research interest is in advanced CMOS devices and their scaling limits. He co-authored a book, "Fundamentals of Modern VLSI Devices," first published in 1998, with the second edition published in 2009.

“SOI Device & Circuits” SOI FUNDAMENTALS CLASS SCHEDULE

- 2:15pm **Welcome & Introduction,**
Samuel Fung, TSMC
- 2:30pm **Fundamentals of SOI MOSFETs: Scaling and Performance**
Yuan Taur, University of California, San Diego
Fundamentals of SOI MOSFETs, scale length model, two region scale length model, minimum channel length of SOI MOSFETs, scaling of partially depleted and fully depleted SOI devices, performance and power advantage of SOI CMOS, and scaling limits of SOI MOSFETs
- 4:00pm **Break**
- 4:15pm **Circuit Design with SOI,**
Andrew Marshall, Texas Instruments Inc.
SOI Components and Device Properties, Passive Components – Resistors, Capacitors, Inductors, Advantages and Disadvantages of SOI, Logic Design in SOI, SOI Memory, SOI Analog Design. Noise Immunity, Electrostatic Discharge (ESD), Reliability, and Low Power Design
- 5:45pm **Closing Remarks**
Samuel Fung, TSMC

ADDITIONAL INFORMATION AND AGENDA

POSTER SESSION - Tuesday, 4:30pm – 6pm

Authors will be available at their posters to answer questions and discuss their work during the Poster Session 4:30pm – 6pm, Tuesday. Posters (without authors) will be on display from Tuesday, 6pm until Thursday, 12pm.

EVENING PANEL - Wednesday, 8pm

Issues and Opportunities in Circuit Design Bulk vs PDSOI vs FDSOI

This exciting and controversial panel session will focus on the issues and highlight the opportunities for Bulk, PDSOI, and FDSOI circuit design. PDSOI and FDSOI proponents claim significant benefits for power and performance compared to bulk circuit designs. However, mainstream circuit designers are hesitant to transition from well-established bulk designs to SOI. Come hear what experts have to say on this topic. Audience participation is encouraged!

Something New! We anticipate this subject to be so interesting that we are opening up the event to people who are not registered for the full conference. For non-attendees who wish to attend the casual dinner, network with conference attendees, and join in the Evening Panel discussion, they may purchase a single event ticket for \$99. If you have a colleague who can not attend the full conference, but would like to attend an evening of SOI and networking, you may purchase an additional ticket on your conference registration form.

Extra tickets for this event **MUST** be purchased in advance. If you do not plan to attend the conference, but would like to attend the Wednesday evening networking dinner and Evening Panel, just complete the conference registration form, but only mark & pay for the Evening Panel.

Please note that the Wednesday night events (Networking Dinner and Evening Panel) are included with full conference registration. You only need to purchase a separate ticket for Wednesday night if you **DO NOT** register for the full conference. The Evening Panel ticket includes dinner as well as entrance to the discussion which follows.

LATE NEWS – Thursday, 3:30pm

Submission for the Late News Session will be accepted until August 24, 2009 and presentation of selected late papers will be on Thursday afternoon. Late News papers are not eligible for either the Best Paper Award or Best Student Award.

NEW - BEST OF CONFERENCE AWARDS

In addition to the traditional Best Paper Award given to the best oral presentation of the conference, the conference will for the first time recognize the best paper authored & presented by a student with a separate award. The Best Student Paper will be selected by the conference committee and presented, along with the Best Paper Award, at the close of the conference.

WELCOME RECEPTION

Monday, 6:00pm

Please join us for the kick-off event of the conference and meet your fellow attendees, presenters, and instructors. We have planned an evening of wine, cheese, and good company - all we'll need is you to make it complete!

CONFERENCE BANQUET

Tuesday, 7:00pm

In addition to a delicious dinner and good company, Douglas C. Maclise of NASA will give a talk entitled "NASA Avionics, the path we've followed and where we're going." He will present a brief history of NASA, the role of electronics, and talk about where NASA is going next.

NETWORKING DINNER

Wednesday, 6:30pm

Combine great food in a casual atmosphere and you have the conference Networking Dinner - and a great way to prepare for the Evening Panel Discussion to follow.

INCLUDED MEALS

Short Course attendees receive a continental breakfast and lunch on Monday and are invited to attend Monday evening's Welcome Reception.

Conference attendees receive a continental breakfast and dinner on both Tuesday and Wednesday, as well as a continental breakfast on Thursday.

AREA AND ACTIVITIES

LOCATION

Silicon Valley is the southern part of the San Francisco Bay Area in Northern California. Silicon Valley continues to be the leading high-tech hub because of the concentration of high-tech companies, manufacturers, and venture capitalists. Foster City sits at the Northern edge of Silicon Valley offering easy access to all of the area's industries and attractions as well as downtown San Francisco.

WEATHER

Foster City, CA climate is mild during summer when temperatures tend to be in the 60's although it can reach the mid-70's. However, like San Francisco, Foster City sits on the bay, so you should be prepared for a change in weather. Dressing in layers is recommended and you should always bring a sweater or jacket!

WEDNESDAY AFTERNOON

ACTIVITIES *(optional)*

If you do not plan to attend the optional Fundamentals Class, your Wednesday afternoon is free time. Take the BART into San Francisco, check with the hotel's concierge about great things to do in the Bay Area, or just lounge around the hotel

AIRPORTS AND TRANSPORTATION

AIRPORTS

The following airports serve the Crowne Plaza Foster City:

San Francisco International (SFO)

- Distance: 7 MI / 11.27 KM South to Hotel
- Complimentary Airport Shuttle
- Taxi Charge (one way): \$40 (USD)
- Time by taxi: 15 MIN

Oakland Airport (OAK)

- Distance: 22 MI / 35.4 KM South West to Hotel
- Taxi Charge (one way): \$60 (USD)
- Time by taxi: 30 MIN

San Jose (SJC)

- Distance: 27 MI / 43.45 KM North to Hotel
- Taxi Charge (one way): \$65 (USD)
- Time by taxi: 35 MIN

HOTEL SHUTTLE

The hotel offers a complimentary shuttle to and from San Francisco International Airport (SFO). After you arrive at the airport and pick up your luggage, call the hotel directly at 650.570.5700 and request pick-up any time between 6am and 11pm.

PARKING

Self-parking is free for conference attendees.

DIRECTIONS

Hwy 101 to 92 east, exit Foster City Blvd and make three rights. From across the Bay take Hwy 880 to 92 west (San Mateo Bridge), exit Foster City Blvd. left on Chess Drive.

[CLICK HERE](#) for interactive custom directions

CONFERENCE HOTEL

Crowne Plaza Foster City
1221 Chess Drive Foster City, California 94404
www.crowneplaza.com/sfo-peninsula

The Crowne Plaza Foster City is centrally located on the San Francisco Bay Peninsula between San Francisco, and San Jose 7 miles from San Francisco International Airport and 22 miles from downtown San Francisco. The hotel offers free Internet access (wired and wireless) in guest rooms, free wireless access in the lobby, restaurants, and pool area. There is a complimentary airport shuttle to and from SFO (San Francisco International Airport) and plenty of parking. In addition, the hotel offers a 24 hour business center (with complimentary computer & printer use for guests), an indoor heated pool and whirlpool, as well as a state-of-the-art fitness center.

HOTEL POLICIES

HOTEL RATES

The Crowne Plaza Foster City is pleased to offer the special, discounted rate of \$149 (plus tax) single/double occupancy for conference attendees. This rate is good from Wednesday, September 30th through Tuesday, October 13th. A major credit card or deposit is needed when you make a reservation to guarantee your room.

Please make sure to reserve your room by September 15, 2009 to insure room availability. If you have a problem making a reservation, please contact the Conference Manager for assistance (bobbi@bacminc.com).

PAYMENT

A deposit equal to one night's room rate is required to hold a reservation. Visa, MasterCard, American Express, Discover, Diner's Club, Carte Blanche, and JCB are accepted, as well as personal checks (subject to approval).

OCCUPANCY and TAXES

All room rates are subject to current applicable state and local taxes, which are presently at 8% with \$2.00 tourism fee.

CHECK-IN/OUT TIMES

Check-in time is 3pm and check-out is 12pm. The Front Desk can arrange to check baggage for those arriving early when rooms are unavailable.

HOW TO MAKE A RESERVATION

• VIA INTERNET

A dedicated website has been created for conference attendees to book their sleeping rooms. Attendees are able to make, modify and cancel hotel reservations online, as well as take advantage of amenities or other services offered by the hotel.

[Click here to make your reservation.](#)

• VIA TELEPHONE

650.570.5700

Please reference group code "SOI."

CONFERENCE REGISTRATION

ON-SITE CONFERENCE REGISTRATION SCHEDULE

Sunday, October 4, 2009	6:00pm – 8:00pm
Monday, October 5, 2009.....	7:00am – 5:00pm
Tuesday, October 6, 2009.....	7:00am – 5:00pm
Wednesday, October 7, 2009	7:00am – 12:00pm
Thursday, October 8, 2009	7:00am – 12:00pm

HOW TO REGISTER FOR THE CONFERENCE

Complete the enclosed registration form.
Please fill in all information completely.

Mail or fax your registration form and payment
no later than September 21, 2009 to:

IEEE International SOI Conference
578 Washington Blvd., #350
Marina del Rey, CA 90292

or fax to: 310.305.1038

Telephone registration is not available.

Please remember to include payment with your mailed
or faxed form as only forms accompanied by payment
will be accepted. There are no exceptions. You may pay
for your registration with either check or credit card.

CANCELLATIONS

Cancellation requests must be made in writing to the
conference manager. Refund requests received by Sep-
tember 21, 2009 will receive a refund of registration
fees less a \$50 processing fee. Requests received after
September 21, 2009 will be considered by the commit-
tee. All refunds will be processed after the conference.

TO PAY BY CREDIT CARD

Complete the registration form including the CREDIT
CARD INFORMATION section and either fax it to
310.305.1038 or mail it to:

IEEE International SOI Conference
578 Washington Blvd., #350
Marina del Rey, CA 90292

Please be sure that the credit card information
is complete, legible, and includes your signature.

TO PAY BY CHECK

Complete the registration form
and mail it with your check to:

IEEE International SOI Conference
578 Washington Blvd., #350
Marina del Rey, CA 90292

Please make the check payable to 2009 IEEE SOI Con-
ference. All checks must be drawn on a US bank and in
US funds only. Registration forms received without
payment will not be honored.

BANK - WIRE TRANSFERS

While payment may be made via bank transfer (by
wiring funds), it is discouraged and there is an ad-
ditional \$25 fee per transfer to cover handling costs.
If a bank transfer is necessary, please contact the
Conference Manager at bobbi@bacminc.com for fur-
ther instructions and the appropriate account numbers.



IEEE 2009 INTERNATIONAL SOI CONFERENCE

OCTOBER 5 - 8 • CROWNE PLAZA HOTEL • FOSTER CITY, CALIFORNIA

NAME TO APPEAR ON BADGE	
*LAST NAME, FIRST NAME, MIDDLE INITIAL	
*COMPANY OR AGENCY	
FOR STUDENT REGISTRATION, please give school attending & graduation year	
*PREFERRED MAILING ADDRESS	*MAIL STOP
*CITY/STATE/ZIP/COUNTRY	
*TELEPHONE NUMBER	*FAX NUMBER
*E-MAIL ADDRESS	
IEEE MEMBER NUMBER	
<input type="checkbox"/> Do you have any special needs? YES:	

REGISTRATION FEES

Advance Registration Fees apply to completed forms and payment received by September 21, 2009

Conference	By Sept 21st	After Sept. 21st
IEEE Member	<input type="checkbox"/> \$475	<input type="checkbox"/> \$525 \$ _____
IEEE Member/Student	<input type="checkbox"/> \$230	<input type="checkbox"/> \$265 \$ _____
Non Member	<input type="checkbox"/> \$625	<input type="checkbox"/> \$675 \$ _____
Non Member/Student	<input type="checkbox"/> \$300	<input type="checkbox"/> \$335 \$ _____

Short Course Tutorial

IEEE Member	<input type="checkbox"/> \$400	<input type="checkbox"/> \$425	\$ _____
IEEE Member/Student	<input type="checkbox"/> \$110	<input type="checkbox"/> \$145	\$ _____
Non Member	<input type="checkbox"/> \$450	<input type="checkbox"/> \$500	\$ _____
Non Member/Student	<input type="checkbox"/> \$170	<input type="checkbox"/> \$205	\$ _____

Fundamentals Class Before or after Sept. 21st

IEEE Member	<input type="checkbox"/> \$170	\$ _____
IEEE Member/Student	<input type="checkbox"/> \$50	\$ _____
Non Member	<input type="checkbox"/> \$235	\$ _____
Non Member/Student	<input type="checkbox"/> \$75	\$ _____

Total Registration Fees \$ _____

Additional Purchases

Dinner Guest Tuesday	_____ @ \$50 ea. = \$ _____
Dinner Guest Wednesday	_____ @ \$50 ea. = \$ _____
Non-attendee Wednesday Evening	
Panel Discussion	_____ @ \$99 ea. = \$ _____

(Includes dinner with conference attendees)

Total Additional Fees \$ _____

TOTAL ENCLOSED \$ _____

Payment **must** accompany registration. Registrations without payment will not be accepted. Wire transfers must be approved in advance and are subject to a \$25 fee. No telephone registrations available

* As you want it to appear on the Conference List of Attendees

**Mail check payable to 2009 IEEE SOI Conference
along with this completed form to:
2009 IEEE SOI CONFERENCE
578 Washington Blvd., #350, Marina del Rey, CA 90292**

Please complete the following for credit card payment only:

Charge registration fees to my:

American Express MasterCard VISA Card

CARD NUMBER

EXP. DATE

NAME AS IT APPEARS ON CREDIT CARD (PLEASE PRINT)

CARDHOLDER'S SIGNATURE