



# IEEE 2011 INTERNATIONAL SOI CONFERENCE



**37th ANNUAL CONFERENCE and 17th ANNUAL SHORT COURSE**

Sponsored by the Institute of Electrical and Electronics Engineers, Inc.  
and the Electron Devices Society

## OCTOBER 3 - 6, 2011

**TEMPE MISSION PALMS HOTEL & CONFERENCE CENTER, TEMPE ARIZONA**

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### QUICK INFORMATION

#### **HOTEL OR ROOM RESERVATION**

Tempe Mission Palms Hotel  
& Conference Center  
60 East 5th Street, Tempe, AZ 85281  
(480) 894-1400  
[www.missionpalms.com](http://www.missionpalms.com)

#### **RESERVATIONS**

[click here](#) for reservations

#### **INTERNATIONAL TRAVELERS**

[click here](#) for information

#### **CONFERENCE OR REGISTRATION QUESTIONS**

Conference Manager  
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6930 De Celis Place #36  
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Fax: 818-855-8392  
[manager@soiconference.org](mailto:manager@soiconference.org)  
[www.soiconference.org](http://www.soiconference.org)

Registration via fax or mail only.

## GENERAL CHAIR'S MESSAGE

On behalf of the Conference Committee, I am pleased to welcome you to the 2011 IEEE International SOI Conference, the leading scientists and engineers interested in all aspects of SOI technology, from materials to devices, from circuits to system applications. The Conference will comprise a three day Technical Program, a Short Course, a Fundamentals Class, and an evening Panel Discussion. In addition, the Conference experience will be enhanced by its location, informal atmosphere and the many social events planned for attendees and their guests.

The Technical Program Committee, chaired by Dr. Jurczak Malgorzata of IMEC, has selected a set of papers that substantially advance the field and highlights the increasing importance of design and technology matching. The invited talks given by specialists and the contributed papers provide the necessary background for users, technologists and product architects.

The conference opens on October 4th with the plenary session containing three talks. Dr. Skotnicki from STMicroelectronics and Dr. Pelloie from ARM will each present the latest advances in FDSOI SOC technology and design. Dr. Yuri Vlasov from IBM will talk about the integration of photonic and electronic devices on SOI.

Other invited talks are embedded into each technical session. They feature world renowned experts in III/V(Ge) on Insulator, GaN on Si, SOI modeling, ultra low power design, memories and SOI specific applications like MEMs, RAD hard and ESD.

This year's hot topic session features four invited talks on FinFET (bulk vs SOI, FinFET variability) and FD/ETSOI.

The theme of the Short Course is "SOI Technology for 15nm SoC." Eight renowned experts in the field will provide a comprehensive overview of requirements for SoC in 15nm node. LSP, LP, HP

technologies, as well as RF and Analog topics will be discussed. FEOL/BEOL/Embedded memory options, 3D Interconnects topic will be covered extensively. The Short Course, organized by Dr. Bich-yen Nguyen SOITEC, will be presented Monday, October 3rd.

On Wednesday afternoon, October 5th, a SOI Fundamentals class is offered. The Fundamentals Class will provide attendees a comprehensive overview of compact device models and the underlying physics of operation for single- and multi-gate FETs.

This educational class, organized by Dr. Makoto Fujiwara of Toshiba, will be instructed by two prominent experts of the SOI community.

Wednesday evening features a cookout and the panel discussion. This year's panel topic is "FinFET." The panel organizer, Dr. Vishal Trivedi of Freescale, has invited distinguished industry experts who will expose their views on FinFET roadmap. We look forward to a lively debate.

Our social program will also include a welcome reception the evening of October 3rd and a banquet dinner on October 4th. Dr. Rakesh Kumar, President & CEO of TCX Technology Connexions, will be our banquet speaker. Dr. Kumar's talk is entitled "Fabless Semiconductors...enabling a wealth of Opportunities." He will discuss the rise of Fabless companies and the challenges they are facing.

I would like to acknowledge the hard work and dedication of the executive and technical committees, as well as the conference management team, for putting together this excellent program. More importantly, let me express my deep appreciation to the authors who submitted papers; their efforts and dedication is at the core of the Conference, which provides a significant yearly contribution to the progress of SOI technology.

—Sincerely, Wade Xiong, General Chair

## EXECUTIVE COMMITTEE

### GENERAL CHAIR

Wade Xiong, AMD GmbH  
[wade.xiong@amd.com](mailto:wade.xiong@amd.com)

**Weize (Wade) Xiong** received his PhD in electrical engineering from University of California, Davis in 2001. Prior to graduate study, he was with Texas Instruments from 1995-1997 as product engineer. From 2000-2002, he led Cypress Semi-Conductor's 90nm low power CMOS transistor development. He returned to TI in 2003. From 2003 to 2006 he was in charge of multi-gate transistors and Nano-wire transistors research evaluations. From 2007 to 2010 Wade led TI's 28nm node low power CMOS transistor development. He also served as manager of SEMATECH Emerging Technology department from 2010 to 2011 and is currently with AMD. Dr. Xiong has authored and co-authored over 80 journal/conference papers, a book chapter on multi-gate MOSFET technologies and holds 27 patents.

He is a senior member of IEEE. He has served on technical committees at the VLSI Technology Symposium and the executive committee of IEEE international SOI conference.

### TECHNICAL PROGRAM CHAIR

Malgorzata Jurczak, imec  
[jurczakm@imec.be](mailto:jurczakm@imec.be)

**Malgorzata Jurczak** has been a manager of Emerging Memories Program at IMEC, Belgium, since 2008. In parallel, in years 2008-2010 she was also a manager of NVM program. Before turning her interests and activities toward the memories, she dedicated the first ten years of her professional carrier to CMOS logic devices.

She received her MSc and PhD in electrical engineering from the Warsaw University of Technology in 1991 and 1997, respectively. After graduation, in parallel with the study toward her PhD she worked as a Professor Assistant in the Institute of Microelectronics and Optoelectronics of Warsaw University of Technology, Warsaw, Poland until 1998. In years 1998-1999 she worked on 0.18 and 0.12 $\mu$ m CMOS and alternative CMOS approaches (strained Si, vertical FET, SON) at CNET, France Telecom, in GRESSI consortium (ST, LETI and CNET). In 2000 she joined IMEC where initially she was leading the IMEC-Philips JDP on 90nm and 65nm CMOS. From 2003 to 2007 she was the manager of IIAP EMERALD program addressing design and fabrication of FINFET devices.

She holds 19 patents, and has authored and co-authored more than 400 publications. She has been a member of scientific committees of IEDM, IEEE SOI, ESSDERC, VLSI TSA conferences and ITRS Roadmap.

### LOCAL ARRANGEMENTS CHAIR

Jean-Luc Pelloie, ARM  
[jean-luc.pelloie@arm.com](mailto:jean-luc.pelloie@arm.com)

**Jean-Luc Pelloie** co-founded SOISIC in April 2001, the first independent company offering SOI IP blocks such as libraries of standard cells, I/Ocells, and memory compilers. He joined ARM at the end of 2006 as Director of SOI Technology as a result of SOISIC's acquisition and has become an ARM Fellow since then.

He received his PhD degree in 1984 from the Institut National des Sciences Appliquées de Lyon. He managed for more than 10 years the SOI CMOS developments at LETI (Grenoble-France) where several technology generations were developed from 1.2  $\mu$ m down to 90 nm. He worked for one year at the IBM Watson Research Center to manage an IBM/LETI SOI program in 93/94 and managed a TI/LETI program for advanced SOI CMOS. His SOI expertise covers both fully-depleted and partially-depleted transistor architectures, including process integration, electrical characterization, Spice modeling and circuit design at transistor level. He has authored and co-authored more than 100 technical papers and is regularly invited to give presentations at renowned international conferences.

He is currently contributing to the Physical IP development on the most advanced SOI process nodes.

## **EXECUTIVE COMMITTEE** continued

### **TREASURER/REGISTRATION CHAIR**

**Bruce Doris, IBM Research**  
[bdoris@us.ibm.com](mailto:bdoris@us.ibm.com)

**Bruce Doris** joined IBM Microelectronics in 1997 where he has held various positions including Process Development and Device Integration. In 2001 he moved to the Exploratory Device Group at IBM Research where he made significant contributions in the areas of Extremely Scaled Transistors, Local Mechanical Stress Technology and Alternate Device Architectures. In 2007 he moved to Albany, NY, to manage the Device Integration Research department at IBM at Albany Nanotech. He has authored or co-authored over 100 papers and holds well over 150 US patents.

### **PUBLICITY & DEVELOPMENT CHAIR**

**Carlos Mazure, Soitec**  
[carlos.mazure@soitec.com](mailto:carlos.mazure@soitec.com)

**Carlos Mazure** is Chief Technology Officer and Executive Vice President of Soitec Group. He joined Soitec in 2001.

Prior to joining Soitec, Dr. Mazure worked for Infineon Technologies in Munich, Germany, where he headed the ferroelectric FeRAM development program. Later, as Director of Business Development at Infineon he initiated the Infineon–Toshiba FeRAM Development Alliance. Before moving to Germany, he worked for the IBM/Infineon DRAM Development Alliance in East Fishkill, New York.

His experience also includes work on SOI, BiCMOS high performance SRAM and technology development at APRDL, Motorola Semiconductor in Austin, Texas.

Mazure holds two doctorates in physics, one from the Grenoble University, France, and the other from the Technical University of Munich, Germany. He has authored or co-authored more than 150 technical papers and holds more than 90 patents worldwide. He is a member of the Semiconductor Advisory Board of Virginia Tech, a member of several international technology and advisory committees, IEEE senior member and a regular invited speaker at international conferences and workshops.

## SENIOR COMMITTEE

### RUMP/POSTER CHAIR

**Vishal Trivedi, Freescale**  
[vishal.p.trivedi@freescale.com](mailto:vishal.p.trivedi@freescale.com)

**Vishal Trivedi** received his PhD in electrical engineering from University of Florida in 2005. His PhD work focused on FD/SOI MOSFET scaling, finFET design with gate-source underlap, generalized threshold-voltage model for doublegate MOSFETs, and quantum-mechanics-based mobility and threshold voltage modeling, and it was incorporated in the physics based compact model UFDG. In 2005, he joined Freescale Semiconductor in Austin, TX, developing high-performance 65nm/45nm PD/SOI CMOS. He successfully integrated milli-second laser spike anneal (with and without the “conventional” spike anneal) in the high-performance CMOS flow. In 2007, he received the Best Paper Award at the IEEE International SOI Conference. Currently, he is with Freescale’s RF Sensors group, developing Si-based millimeter-wave (30GHz-300GHz) technology and design for applications such as 76-81GHz automotive radar. Vishal is the author or co-author of more than 25 papers published in technical journals and conference proceedings. He holds eleven patents and has about ten more pending.

### SHORT COURSE CHAIR

**Bich-Yen Nguyen, Soitec**  
[bich-yen.nguyen@soitec.com](mailto:bich-yen.nguyen@soitec.com)

**Bich-Yen Nguyen** recently joined Soitec as a Senior Fellow representing Soitec’s R&D and supporting the device development and applications for Soitec’s core technologies. Bich-Yen is also responsible for joint device technology development projects with Soitec partners/customers worldwide. Prior to joining Soitec, Bich-Yen was a senior manager at Freescale Semiconductor and a Freescale/Motorola Dan Noble Fellow. Bich-Yen has been recognized for her leadership and research in developing Freescale/Motorola’s CMOS technology for advanced integrated circuit products. She also was instrumental in transferring process technology to production since 1980, which resulted in a competitive market entry position for Freescale/Motorola. Her honors and awards include recipient of Distinguished Innovation award in 1991, Motorola Science Advisory Board Associate in 1992, Dan Noble Fellow in 2001 the highest technical award in Motorola, Master of Innovation Award in 2003. In 2004, she received the 1st National Award “Women in Technology Lifetime Achievement Award.” She holds over 130 worldwide patents and has authored more than 150 technical papers on IC process, integration and device technologies. She gave several invited talks, panel discussions and keynote

speeches at major international conferences and universities. She also served as a committee member for IEDM, SISC, ECS conferences and currently serves as a steering and technical committee member of the International Conference on Integrated Circuit Design and Technology.

### FUNDAMENTALS CLASS CHAIR

**Makoto Fujiwara, Toshiba**  
[makoto.fujiwara@toshiba.co.jp](mailto:makoto.fujiwara@toshiba.co.jp)

**Makoto Fujiwara** received his BS degree in electrical engineering from North Carolina State University, Raleigh, NC in 1992 and his MS degree in electrical engineering from Stanford University, Stanford, CA in 1994. He was a research and teaching assistant at Stanford University in 1995. He joined Toshiba Corporation in 1996 where he was responsible for device design and process integration of both bulk and SOI MOSFETs, device/process modeling for TCAD, and development of advanced gate stack. From 2005 to 2006, he was a visiting researcher at Stanford University where he worked on physics and modeling of high mobility channel devices. In 2006, he returned to Toshiba Corporation and engaged in device design and integration for 28/20 nm node logic technology. Since 2008, he has been with IBM Toshiba System LSI Development Alliance in Albany, NY, conducting development and evaluation of low power CMOS technologies.

## **SENIOR COMMITTEE** continued

### **MULTIMEDIA CHAIR**

**Olivier Faynot, CEA-LETI**  
[olivier.faynot@cea.fr](mailto:olivier.faynot@cea.fr)

**Olivier Faynot** received his MSc and PhD degrees from the Institut National Polytechnique de Grenoble, France in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron Fully Depleted SOI devices fabricated on ultrathin SIMOX wafers.

He joined LETI (CEA-Grenoble, France) in 1995, working on simulation and modeling of deep submicron fully and partially depleted SOI

devices. His main activity was the development of a dedicated Partially Depleted SOI SPICE model, called LETISOI. From 2000 to 2002, he was involved in the development of a sub 0.1 $\mu$ m partially depleted technology. From 2003 to 2007, he was leading the development of advanced single and multiple-gate Fully Depleted SOI technologies with High K and Metal gate. From 2008 to 2010, he managed the innovative devices laboratory at LETI. Since 2011, he is responsible of the Microelectronic component section at LETI.

He is author and co-author of more than 140 scientific publications on SOI in journals and international conferences. Since 2001, Dr. Faynot was successively in the committees of the main international conferences like International Electron Device Meeting (IEDM), the symposium on VLSI Technology, the IEEE International SOI conference, the EUROSOI workshop, and the Solid State Device and Materials (SSDM) conference.

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## CONFERENCE AT-A-GLANCE

### MONDAY, October 3rd

- 7:00am **Short Course Breakfast**
- 8:00am Short Course
- 12:30pm Short Course Lunch
- 1:30pm Short Course
- 6:00pm **Welcome Reception**

### TUESDAY, October 4th

- 7:00am **Continental Breakfast**
- 8:00am Introduction & Welcome
- 8:15am Session 1: PLENARY SESSION
- 10:15am **Break**
- 10:30am Session 2: FINFET AND NANOWIRES
- 12:10pm **Lunch** (on own)
- 1:10pm Session 3: FD SOI DEVICES
- 4:05pm Break
- 4:25pm Session 4: POSTERS
- 7:00pm **Banquet**

### WEDNESDAY, October 5th

- 7:00am **Continental Breakfast**
- 8:00am Session 5: III-V AND NEW DEVICES
- 10:30am **Break**
- 10:45am Session 6: MATERIALS AND SUBSTRATE ENGINEERING
- 12:30pm **Lunch & Free time** (on own)
- 1:15pm FUNDAMENTALS CLASS: "Fundamental Physics and Compact Models for Single-gate SOI and Multi-gate FETs" (optional)
- 6:30pm **Cookout**
- 8:00pm Evening Panel Discussion: "FinFETs"

### THURSDAY, October 6th

- 7:00am **Continental Breakfast**
- 8:00am Session 7: HOT TOPICS
- 9:40pm **Break**
- 9:55am Session 8: ESD AND RADHARD DEVICES AND SOI CIRCUITS
- 11:45am **Lunch** (on own)
- 12:45pm Session 9: MEMORIES
- 2:15pm **Break**
- 2:30pm Session 10: MEMS AND SENSORS
- 3:35pm Session 11: LATE NEWS
- 4:35pm **Break**
- 5pm Wrap-up & Presentation of Best Paper & Best Student Paper Awards

### INCLUDED MEALS

**Short Course attendees** receive a continental breakfast and lunch on the day of the Course, Monday, and are invited to attend Monday evening's Welcome Reception.

**Conference attendees** receive a continental breakfast and dinner on both Tuesday and Wednesday, as well as a continental breakfast on Thursday.

## TECHNICAL SESSIONS

THE TECHNICAL PROGRAM will consist of 26 oral and 11 poster papers, as well as 18 invited talks. Technical Sessions and Session Chairs are as follows:

- |                  |  |                   |   |
|------------------|--|-------------------|---|
| <b>SESSION 1</b> | Plenary<br>Wade Xiong, Gosia Jurczak                                 | <b>SESSION 7</b>  | Hot Topics<br>Carlos Mazure, Samuel Fung                                    |
| <b>SESSION 2</b> | FinFET and Nanowires<br>Meishoku Massahara, Tsu Jae King             | <b>SESSION 8</b>  | ESD and RadHard Devices<br>and SOI Circuits<br>Jean-Luc Pelloie, Les Pakuli |
| <b>SESSION 3</b> | FD SOI Devices<br>Bruce Doris, Olivier Faynot                        | <b>SESSION 9</b>  | Memories<br>Gary Bronner, Geng Wang   |
| <b>SESSION 4</b> | Posters<br>Denis Flandre, Tom Hill                                   | <b>SESSION 10</b> | MEMS and Sensors<br>Chang Lee Chen, Jeremy Popp                             |
| <b>SESSION 5</b> | III-V and New Devices<br>Nobuyuki Sugii, Toshiro Hiramoto            | <b>SESSION 11</b> | LATE NEWS<br>Uygar Avici, Frederic Ganesello                                |
| <b>SESSION 6</b> | Materials and Substrate Engineering<br>Frank Fournel, Horacio Mendez |                   |   |

## TECHNICAL PROGRAM SCHEDULE

- |                  |   |
|------------------|---|
| <b>SESSION 1</b> | Plenary   |
| 8:15am           | 1.1 <b>Competitive SOC on UTBB SOI</b><br>T. Skotnicki; <i>ST Microelectronics (invited)</i>  |
| 8:55am           | 1.2 <b>FDSOI Design Portability from BULK at 20nm Node</b><br>J.L. Pelloie; <i>ARM (invited)</i>  |
| 9:35am           | 1.3 <b>Integration of Photonics and Electronic Circuits on Common SOI Platform</b><br>Y. Vlasov, <i>IBM (invited)</i>   |
| <b>SESSION 2</b> | FinFET and Nanowires  |
| 10:30am          | 2.1 <b>Analysis of Parasitic Resistance in Double Gate FinFETs with Different Fin Lengths</b><br>X.Yang <sup>1</sup> , K. Maitra <sup>1</sup> , C. Yeh <sup>2</sup> , P. Zeitzoff <sup>3</sup> , M. Raymond <sup>1</sup> , P. Kulkarni <sup>2</sup> , M. Wang <sup>2</sup> ,<br>T. Yamashita <sup>2</sup> , V. S. Basker <sup>2</sup> , T.E. Standaert <sup>2</sup> , S. Samavedam <sup>4</sup> , H. Bu <sup>2</sup> , R.J. Miller <sup>1</sup> ;<br><sup>1</sup> GLOBALFOUNDRIES Inc., Albany, <sup>2</sup> IBM Research, <sup>3</sup> Toshiba,<br><sup>4</sup> GLOBALFOUNDRIES, Inc., Hopewell Junction |

## TECHNICAL PROGRAM SCHEDULE continued

- 10:50am 2.2 **Influence of Fin Height on Poly-Si/PVD-TiN Stacked Gate FinFET Performance**  
T. Hayashida<sup>1,2</sup>, K. Endo<sup>3</sup>, Y.X. Liu<sup>3</sup>, S. O'uchi<sup>3</sup>, T. Matsukawa<sup>3</sup>, W. Mizubayashi<sup>3</sup>,  
S. Migita<sup>3</sup>, Y. Morita<sup>3</sup>, H. Ota<sup>3</sup>, H. Hashiguchi<sup>1</sup>, D. Kosemura<sup>1</sup>, T. Kamei<sup>1</sup>, J. Tsukada<sup>3</sup>,  
Y. Ishikawa<sup>3</sup>, H. Yamauchi<sup>3</sup>, A. Ogura<sup>1</sup>, and M. Masahara<sup>1,3</sup>; <sup>1</sup>*School of Science and  
Technology, Meiji University*, <sup>2</sup>*Research Fellow of the Japan Society for the Promotion  
of Science*, <sup>3</sup>*National Institute of AIST*
- 11:10am 2.3 **Impacts of Single Trap Induced Random Telegraph Noise on FinFET Devices and  
SRAM Cell Stability**  
M.L. Fan, V.P.H. Hu, Y.N. Chen, P. Su, C.T. Chuang; *Department of Electronics Engineering &  
Institute of Electronics, National Chiao Tung University*
- 11:30am 2.4 **Uniaxial Stress Efficiency for Different Fin Dimensions of Triple-Gate SOI nMOSFETs**  
R. T. Bühler<sup>1</sup>, P. G. D. Agopian<sup>1,2</sup>, R. Giacomini<sup>1,2</sup>, E. Simoen<sup>3</sup>, C. Claeys<sup>3,4</sup>, J.A. Martino<sup>1</sup>;  
<sup>1</sup>*LSI/PSI/USP, University of Sao Paulo*, <sup>2</sup>*FEI*, <sup>3</sup>*imec*, <sup>4</sup>*E.E. Dept., KU Leuven*
- 11:50am 2.5 **Random Dopant Variation in Junctionless Nanowire Transistors**  
N. D. Akhavan, I. Ferain, P. Razavi, R.Y. and J.P. Colinge Tyndall;  
*National Institute, University College, Cork*
- SESSION 3** **FD SOI Devices**
- 1:10pm 3.1 **Implant Approaches and Challenges for 20nm Node and Beyond ETSOI Devices**  
S. Ponoth<sup>1</sup>, M. Vinet<sup>1</sup>, L. Grenouillet<sup>2</sup>, A. Kumar<sup>1</sup>, P. Kulkarni<sup>1</sup>, Q. Liu<sup>3</sup>, K. Cheng<sup>1</sup>, B. Haran<sup>1</sup>,  
N. Possémé<sup>2</sup>, A. Khakifirooz<sup>1</sup>, N. Loubet<sup>3</sup>, S. Mehta<sup>1</sup>, J. Kuss<sup>1</sup>, V. Destefanis<sup>2</sup>, N. Berliner<sup>1</sup>,  
R. Sreenivasan<sup>1</sup>, Y. Le Tiec<sup>2</sup>, S. Kanakasabapathy<sup>1</sup>, S. Schmitz<sup>1</sup>, T. Levin<sup>1</sup>, S. Luning<sup>4</sup>, T. Hook<sup>1</sup>,  
M. Khare<sup>1</sup>, G. Shahidi<sup>1</sup>, B. Doris<sup>1</sup>; <sup>1</sup>*IBM*, <sup>2</sup>*CEA-LETI*, <sup>3</sup>*ST Microelectronics*,  
<sup>4</sup>*GLOBALFOUNDRIES, Albany NanoTech*
- 1:30pm 3.2 **Statistical Variability in N-Channel UTB-FD-SOI MOSFETs Under the Influence of  
RDF, LER, MGG and PBTI**  
S. Markov<sup>1</sup>, N.M. Idris<sup>1</sup>, A. Asenov<sup>1,2</sup>; <sup>1</sup>*Device Modelling Group, School of Engineering, Uni-  
versity of Glasgow*, <sup>2</sup>*Gold Standard Simulations Ltd (GSS)*
- 1:50pm 3.3 **Properties of 22nm Node Extremely-thin-SOI MOSFETs**  
N. Rodriguez<sup>1</sup>, F. Andrieu<sup>2</sup>, C. Navarro<sup>1</sup>, O. Faynot<sup>2</sup>, F. Gamiz<sup>1</sup>, S. Cristoloveanu<sup>3</sup>;  
<sup>1</sup>*Dept. Electronics, University of Granada*, <sup>2</sup>*CEA-LETI*, <sup>3</sup>*IMEP-INP Grenoble MINATEC*
- 2:10pm 3.4 **Surface Potential Based Model of Ultra-Thin Fully Depleted SOI MOSFET for IC Simulations**  
M.A. Jaud; *CEA-LETI (invited)*
- 2:35pm 3.5 **An Exercise of ET/UTBB SOI CMOS Modeling and Simulation with BSIM-IMG**  
Q. Chen<sup>1</sup>, X.Zhong<sup>1</sup>, Y.Wu<sup>1</sup>, N.Zhu<sup>1</sup>, W.Huang<sup>1</sup>, D. Lu<sup>2</sup>, C. Hu<sup>2</sup>, B.Y. Nguyen<sup>3</sup>,  
O. Faynot<sup>4</sup>; <sup>1</sup>*Accelicon Technologies Inc.*, <sup>2</sup>*University of California, Berkeley*,  
<sup>3</sup>*Soitec*, <sup>4</sup>*CEA-LETI (invited)*

## TECHNICAL PROGRAM SCHEDULE continued

- 3:00pm 3.6 **TCAD Study of Back-gate Biasing in UTBB**  
T.B. Hook<sup>1</sup>, S. Furkay<sup>1</sup>, P. Kulkarni<sup>2</sup>, F. Monsieur<sup>3</sup>; <sup>1</sup>IBM SRDC, <sup>2</sup>IBM Albany NanoTech, <sup>3</sup>ST Microelectronics, Albany NanoTech
- 3:20pm 3.7 **Self-Heating Effects in Ultrathin FD SOI Transistors**  
N. Rodriguez<sup>1</sup>, C. Navarro<sup>1</sup>, F. Andrieu<sup>2</sup>, O. Faynot<sup>2</sup>, F. Gamiz<sup>1</sup>, S. Cristoloveanu<sup>3</sup>;  
<sup>1</sup>Dept. Electronics, University of Granada, <sup>2</sup>CEA-LETI, <sup>3</sup>IMEP-INP Grenoble MINATEC
- 3:40pm 3.8 **Road to V<sub>min</sub>=0.4V LSIs with Least-Variability FDSOI and Back-Bias Control**  
N. Sugii; *LEAP (invited)*

### SESSION 4

#### Posters

- 4:25pm 4.1 **Method for Direct Characterizing Interface Traps in STI-type High Voltage SOI LDMOSFETs**  
Y. He, G. Zhang; *Institute of Microelectronics and Key Laboratory of Microelectronics Devices and Circuits, Peking University*
- 4.2 **Ultra-Thin SOI for 20nm Node and Beyond**  
C. Aulnette<sup>1</sup>, W. Schwarzenbach<sup>1</sup>, N. Daval<sup>1</sup>, O. Bonnin<sup>1</sup>, B.Y. Nguyen<sup>1</sup>, C. Mazure<sup>1</sup>,  
C. Maleville<sup>1</sup>, K. Cheng<sup>2</sup>, S. Ponoth<sup>2</sup>, A. Khakifirooz<sup>2</sup>, T. Hook<sup>2</sup>, B. Doris<sup>2</sup>; <sup>1</sup>SOITEC,  
<sup>2</sup>IBM Research at Albany Nanotech Center
- 4.3 **Investigation of Hole Mobility in Ultrathin-Body SOI MOSFETs on (110) Surface: Effects of Silicon Thickness and Body Doping**  
M. Poljak<sup>1</sup>, V. Jovanovi<sup>2</sup>, T. Suligoj<sup>1</sup>; <sup>1</sup>FER-ZEMRIS, University of Zagreb, <sup>2</sup>DIMES, Delft University of Technology
- 4.4 **1/f Noise Measurements of Bonded SOS and Epi SOS Fully-Depleted MOSFETs to 10 MHz**  
L.W. Chen, J.W. Roach, F.M. Rotella; *Peregrine Semiconductor Corp.*
- 4.5 **High-Q FDSOI Varactors for Wireless Radiation Sensing**  
G. Vaidhyanathan, S.J. Koester; *Department of Electrical Engineering, University of Minnesota-Twin Cities*
- 4.6 **Charge Sensitive Amplifier Study in 2um FD SOI CMOS**  
L.S. Yee, E. Martin, E. Cortina, C. Renaux, D. Flandre; *Université catholique de Louvain*
- 4.7 **ESD Considerations for SOI Switch Design**  
Y.Y. Chen, T.Y. Lee, E. Lawrence, J. Woods; *Skyworks Solutions, Inc.*
- 4.8 **SOI MESFETs for Extreme Environment Buck Regulators**  
W. Lepkowski<sup>1,2</sup>, M. Goryll<sup>1</sup>, S.J. Wilk<sup>1,2</sup>, Y. Zhang<sup>1</sup>, J. Sochacki<sup>1</sup>, T.J. Thornton<sup>1,2</sup>;  
<sup>1</sup>Arizona State University, <sup>2</sup>SJT Micropower Inc.

## TECHNICAL PROGRAM SCHEDULE continued

4.9 **Pre-Silicon 22/20nm Compact MOSFET Models for Bulk vs. FD SOI Low-Power Circuit Benchmarks**

D. Bol, S. Bernard, D. Flandre; *ICTEAM Institute, Université catholique de Louvain*

4.10 **Analysis of the Low-Frequency Noise of Junctionless Nanowire Transistors Operating in Saturation**

R.T. Doria<sup>1</sup>, R.D. Trevisoli<sup>2</sup>, M. de Souza<sup>1</sup>, J.P. Colinge<sup>3</sup>, M.A. Pavanello<sup>1,2</sup>;

<sup>1</sup>Electrical Engineering Department, Centro Universitário da FEI, <sup>2</sup>LSI/PSI/USP, University of São Paulo, <sup>3</sup>Tyndall National Institute, UCC – Lee Maltings

4.11 **Millimeter-Wave Power Amplifiers in 45nm CMOS SOI Technology**

J.H. Chen, S.R. Helmi, S. Mohammadi; *Purdue University*

### SESSION 5

#### III-V and New Devices

8:00am

5.1 **(III-V/Ge)-on-Insulator CMOS Technology**

S. Takagi; *University of Tokyo (invited)*

8:25am

5.2 **A Proposed High Manufacturability Strain Technology for High-k/Metal Gate SiGe-SOI CMOSFET**

W.K. Yeh<sup>1</sup>, C.Y. Cheng<sup>1</sup>, Y.L. Yang<sup>2</sup>, C.T. Lin<sup>3</sup>, C.M. Lai<sup>3</sup>, Y.W. Chen<sup>3</sup>, C. H. Hsu<sup>3</sup>, C.W. Yang<sup>3</sup>, P.Y. Chen<sup>4</sup>; <sup>1</sup>Department of Electrical Engineering, National University of Kaohsiung, <sup>2</sup>National Kaohsiung Normal University, <sup>3</sup>Central R&D Division, <sup>4</sup>UMC, I-Shou University

8:45am

5.3 **Features of Electron Mobility in Ultrathin-Body InGaAs-On-Insulator MOSFETs Down to Body Thickness of 2nm**

M. Poljak<sup>1</sup>, V. Jovanovi<sup>2</sup>, T. Suligoj<sup>1</sup>; <sup>1</sup>FER-ZEMRIS, University of Zagreb, <sup>2</sup>DIMES, Delft University of Technology

9:05am

5.4 **Assessment of III-V MOSFET Architectures for Low Power Applications Using Static and Dynamic Numerical Simulation**

M. Shi<sup>1</sup>, J. Saint-Martin<sup>1</sup>, A. Bournel<sup>1</sup>, D. Querlioz<sup>1</sup>, P. Dollfus<sup>1</sup>, J. Mo<sup>2</sup>, N. Wichmann<sup>2</sup>, L. Desplanque<sup>2</sup>, X. Wallart<sup>2</sup>, F. Danneville<sup>2</sup>, S. Bollaert<sup>2</sup>; <sup>1</sup>IEF, CNRS, Univ. Paris Sud, <sup>2</sup>IEMN, CNRS / Univ. Lille1

9:25am

5.5 **Steep Subthreshold Slope Devices on SOI**

T.J. King, P. Matheu, Z. Jacobson, S. H. Kim; *University of California, Berkeley (invited)*

9:50am

5.6 **Anomalous Floating-Body Effects in SOI MOSFETs: Low-Voltage CMOS?**

J.G. Fossum, Z. Lu; *University of Florida*

10:10am

5.7 **Novel Architecture to Boost the Vertical Tunneling in Tunnel Field Effect Transistors**

D. Leonelli<sup>1,2</sup>, A. Vandooren<sup>1</sup>, R. Rooyackers<sup>1</sup>, A.S. Verhulst<sup>1</sup>, C. Huyghebaert<sup>1</sup>, S. De Gendt<sup>1,3</sup>, M.M. Heyns<sup>1,4</sup>, G. Groeseneken<sup>1,2</sup>; <sup>1</sup>Imec, <sup>2</sup>Katholieke Universiteit Leuven, ESAT, Department of Electric Engineering, <sup>3</sup>Katholieke Universiteit Leuven, Chemistry Department, <sup>4</sup>Katholieke Universiteit Leuven, Department of Metallurgy and Materials Engineering

## TECHNICAL PROGRAM SCHEDULE continued

- SESSION 6**      **Materials and Substrate Engineering**
- 10:45am      6.1 **Integration of Gallium Nitride and Silicon: From Devices to Diamond**  
E. Piner; *Texas State University (invited)*
- 11:10am      6.2 **Strain Reduction in Silicon-on-Sapphire by Wafer Bonding**  
G.P. Imthurn<sup>1</sup>, A.M. Miscione<sup>1</sup>, K. Landry<sup>2</sup>, A. Vaufredaz<sup>2</sup>, T. Barge<sup>2</sup>, C. Lagahe-Blanchard<sup>2</sup>  
<sup>1</sup>Peregrine Semiconductor Corporation, <sup>2</sup>Soitec
- 11:30am      6.3 **Low-Temperature Properties of ZnO on Insulator MOSFETs**  
S.J. Chang<sup>1</sup>, M. Bawedin<sup>2</sup>, B. Bayraktaroglu<sup>3</sup>, J.H. Lee<sup>4</sup>, S. Cristoloveanu<sup>1</sup>; <sup>1</sup>IMEP-LAHC (UMR 5130), Grenoble INP Minatec, <sup>2</sup>IES, University of Montpellier <sup>2,3</sup>AFRL/RD, OH 45433, <sup>4</sup>Kyungpook National University
- 11:50am      6.4 **Mobility Profiles and Thermal Characterization of SOI and Si-on-SiC Hybrid Substrates**  
S. Lotfi, L.G. Li, Ö. Vallin, H. Norström, J. Olsson; *Uppsala University, The Ångström Laboratory, Solid State Electronics*
- 12:10pm      6.5 **Ellipsometry Measurements on Ultrathin Silicon on Insulator Films**  
L. Grenouillet<sup>1</sup>, Y. Le Tiec<sup>1</sup>, Q. B. Vu<sup>2</sup>, M. Vinet<sup>1</sup>, J. D. LaRose<sup>3</sup>, V. K. Kamineni<sup>3</sup>, N. Posseme<sup>1</sup>, J. Fullam<sup>2</sup>, B.B. Doris<sup>2</sup>, A. C. Diebold<sup>3</sup>; <sup>1</sup>CEA-LETI, <sup>2</sup>IBM, <sup>3</sup>College of Nanoscale Science & Engineering
- SESSION 7**      **Hot Topics**
- 8:00am      7.1 **Benefits and Challenges of FDSOI Technology for 14nm Node**  
O. Faynot; *CEA-LETI (invited)*
- 8:25am      7.2 **The Future of SOI Transistor Technology**  
B. Doris; *IBM (invited)*
- 8:50am      7.3 **FinFET Technology: A Substrate Perspective**  
H. Bu; *IBM (invited)*
- 9:15am      7.4 **Variability Origins of FinFETs and Perspective Beyond 20nm Node**  
T. Matsukawa; *AIST (invited)*
- SESSION 8**      **ESD and RadHard Devices and SOI Circuits**
- 9:55am      8.1 **Radiation Hardness of FDSOI and FinFET Technologies**  
M. Alles; *Vanderbilt University (invited)*
- 10:20am      8.2 **ESD Protection in FinFET Technologies**  
S. Thijs; *IMEC (invited)*

## TECHNICAL PROGRAM SCHEDULE continued

- 10:45am 8.3 **Asymmetric Self-Cascode Configuration to Improve the Analog Performance of SOI nMOS Transistors**  
M. de Souza<sup>1</sup>, D. Flandre<sup>2</sup>, M.A. Pavanello<sup>1</sup>; <sup>1</sup>Department of Electrical Engineering, Centro Universitário da FEI, <sup>2</sup>Electrical Engineering Department, ICTEAM Institute, Université catholique de Louvain
- 11:05am 8.4 **Comparison of Small-Signal Output Conductance Frequency Dependence in UTBB SOI MOS FETs with and without Ground Plane**  
S. Makovejev<sup>1</sup>, J.P. Raskin<sup>2</sup>, D. Flandre<sup>2</sup>, S. Olsen<sup>1</sup>, F. Andrieu<sup>3</sup>, T. Poiroux<sup>3</sup>, V. Kilchytska<sup>2</sup>; <sup>1</sup>School of Electrical, Electronic and Computer Engineering, Newcastle University, <sup>2</sup>ICTEAM Institute, Université catholique de Louvain, <sup>3</sup>CEA-LETI, MINATEC Campus
- 11:25am 8.5 **Ultra-high-efficiency Co-integrated Photovoltaic Energy Scavenger**  
G. Gosset, O. Bulteel, P. Baijot, D. Flandre; Université catholique de Louvain (UCL), ICTEAM Institute

### SESSION 9

#### Memories

- 12:45pm 9.1 **Novel Memory Ideas using Floating Body Effects**  
J. Cho; Global Foundries (invited)
- 1:10pm 9.2 **BJT Effect Analysis in p- and n-SOI MuGFETs with High-k Gate Dielectrics and TiN Metal Gate Electrode for a 1T-DRAM Application**, M. Galetti<sup>1</sup>, M. Rodrigues<sup>1</sup>, J. A. Martino<sup>1</sup>, N. Collaert<sup>2</sup>, E. Simoen<sup>2</sup>, M. Aoulaiche<sup>2</sup>, M. Jurczak<sup>2</sup>, C. Claeys<sup>2,3</sup>; <sup>1</sup>LSI/PSI/USP, University of Sao Paulo, <sup>2</sup>imec, <sup>3</sup>E.E. Dept., KU Leuven
- 1:30am 9.3 **Comparative Study of Tri-gate Flash Memories with Split and Stack Gates**  
T. Kamei<sup>1</sup>, Y.X. Liu<sup>2</sup>, T. Matsukawa<sup>2</sup>, K. Endo<sup>2</sup>, S.O'uchi<sup>2</sup>, J. Tsukada<sup>2</sup>, H. Yamauchi<sup>2</sup>, Y. Ishikawa<sup>2</sup>, T. Hayashida<sup>1</sup>, K. Sakamoto<sup>2</sup>, A. Ogura<sup>1</sup>, M. Masahara<sup>2</sup>; <sup>1</sup>School of Science and Technology, Meiji University, <sup>2</sup>AIST
- 1:50pm 9.4 **High Density DRAM for Space Utilizing Embedded DRAMs Macros in 32nm SOI CMOS**  
J. Popp; Boeing Research and Technology (invited)

### SESSION 10

#### MEMS and Sensors

- 2:30pm 10.1 **Sensing and MEMS Devices in Thin-Film SOI MOS Technology**  
J.P. Raskin; Université catholique de Louvain (invited)
- 2:55pm 10.2 **Innovative Frequency Output Pressure Sensor with Single SOI nMOSFET Suspended Transducer**  
B. Olbrechts, B. Rue, D. Flandre and J.P. Raskin; Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM) Université catholique de Louvain
- 3:15pm 10.3 **A SOI CMOS Smart Strain Sensor**  
B. Rue, B. Olbrechts, J.P. Raskin, D. Flandre; Institute of Information and Communications Technologies, Electronics and Applied Mathematics (ICTEAM) Université catholique de Louvain

## 17<sup>TH</sup> ANNUAL SHORT COURSE

### “The SOI Technologies for 15nm SoC”

The one-day short course features presentations by industry and academia experts on the process, material and device technology options for 15nm System-on-Chip and their implications. The short course content offers a large perspective on the opportunities which SOI opens in the field of low-power, high-performance CMOS systems-on-chip, with an emphasis on digital, memory, analog and RF functions.

### SHORT COURSE SCHEDULE

Monday, October 3rd

7am	8am	<b>Breakfast</b>
8am	8:10am	<b>Welcome &amp; Introduction</b> , <i>Bich-Yen Nguyen, Soitec</i>
8:10am	9:10am	<b>LP/G/HP SoC Requirement for 15nm</b> , <i>Ali Keshavarzi, Global Foundries</i>
9:10am	10:10am	<b>Materials and Process Technologies for 15nm</b> , <i>Vamsi Paruchuri, IBM</i>
10:10am	10:30am	<b>Break</b>
10:30am	11:30am	<b>Digital Device Architecture and its Implication</b> , <i>Olivier Faynot, CEA-LETI</i>
11:30am	12:30pm	<b>Analog and RF Requirements for Advanced CMOS Nodes: the SOI perspective</b> , <i>Frederic Giancesello, ST Microelectronics</i>
12:30am	1:30pm	<b>Hosted Lunch</b>
1:30pm	2:30 pm	<b>More than Moore: Optical Interconnect and Sensor</b> , <i>Juthika Basak, Intel</i>
2:30pm	3:30pm	<b>3D Interconnect and Packaging technology</b> , <i>Mercha Abdelkarim, IMEC</i>
3:30pm	4:30pm	<b>Memory</b> , <i>Genadi Bersuker, Sematech</i>
4:30pm	4:45pm	<b>Closing Remarks</b>

## 5<sup>TH</sup> ANNUAL SOI FUNDAMENTALS CLASS OVERVIEW

### “Fundamental Physics and Compact Models for Single-gate SOI and Multi-gate FETs”

The **Fundamentals Class** will provide attendees a comprehensive overview of compact device models and the underlying physics of operation for single- and multi-gate FETs. Included in the coverage of the class will be a section on physics-based modeling of single-gate transistors, for both partially-depleted and fully-depleted with a wide range of BOX

thicknesses. The model is based on the potential distribution from the device front surface to the back surface. In this surface-potential-based model, charges induced at different surfaces are efficiently formulated as a function of the potential distribution. The other section will cover a versatile multi-gate compact model. Included will be coverage of relevant

physical effects such as bias-dependent scaling length, thin-body quantum confinement, temperature/self-heating effects and parasitic capacitance. Inclusion of these features realizes a fully scalable model that is capable of investigating multi-gate architectures at the circuit level.

## SOI FUNDAMENTALS CLASS INSTRUCTORS

### MITIKO MIURA-MATTAUSCH

received her DrSc degree from Hiroshima University, Hiroshima, Japan. From 1981, she was a Researcher with the Max-Planck-Institute for solid-state physics in Stuttgart, Germany, where she working with non-linear phenomena in solid state. From 1984 to 1996, she was with Corporate Research and Development, Siemens AG, Munich, Germany, where she worked on hot-electron problems in MOSFETs, the development of bipolar transistors, and analytical modeling of deep sub-micron MOSFETs for circuit simulation. Since 1996 she has been a professor with the Department of Semiconductor Electronics and Integration Science, Graduate School of Advanced Sciences of Matter, Hiroshima University, where she is leading the ultra-scaled devices laboratory and focusing on advanced MOSFETs features under RF opera-

tion as well as MOSFETs with thin active layer experimentally and theoretically. Her important achievement is the development of the compact MOSFET model HiSIM based on the complete surface-potential description, which has been selected as a standard model by the Compact Modeling Council. Dr. Miura-Mattausch is a Fellow and a Distinguished Lecturer of IEEE Electron Device Society.

### CHUNG-HSUN LIN

received his BS and MS degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, ROC, in 1999 and 2001, and the PhD degree in electrical engineering from the University of California, Berkeley, in 2007. He joined the IBM T.J. Watson Research Center in 2008 as a Research Staff Member in the area of CMOS technology development and device modeling for 22nm node

and beyond. His PhD work focused on the compact modeling of non-classical MOSFETs and SOI devices, performance evaluation of advanced CMOS technology, and the impact of process variations on circuits. His current interests include device design and modeling of FinFET, ETSOI, PDSOI, solar cell, and memory.

Dr. Lin is a recipient/co-recipient of the Best Student Paper Award in VLSI-Technology 2007, ICSICT 2006, VLSI-TSA 2005 and ISDRS 2001, and other awards. He has received six IBM Invention Achievement Awards. He has authored or coauthored more than 50 technical papers. He is a sub-committee member in Compact Modeling Council for multi-gate FET model standardization effort. He is currently a Reviewer of the IEEE TRANSACTIONS ON ELECTRON DEVICES and ELECTRON DEVICE LETTERS.

**“Fundamental Physics and Compact Models  
for Single-gate SOI and Multi-gate FETs”  
SOI FUNDAMENTALS CLASS SCHEDULE**

**Wednesday, October 5th, 2011**

- 2:15pm**      **Welcome & Introduction**  
*Makoto Fujiwara, Toshiba America Electronic Components, Inc.  
(USA)*
- 2:25pm**      **Compact Model for Single-gate SOI FET Based on the Potential  
Distribution**  
*Mitiko Miura-Mattausch, Hiroshima University (Japan)*
- 3:55pm**      **Break**
- 4:10pm**      **Compact Model for Multi-gate FET**  
*Chung-Hsun Lin, IBM (USA)*
- 5:40pm**      **Closing Remarks**  
*Makoto Fujiwara, Toshiba America Electronic Components, Inc.  
(USA)*

## **ADDITIONAL INFORMATION AND AGENDA**

### **WELCOME RECEPTION • Monday, 6:00pm**

You are cordially invited to join us as we kick off our 2011 Conference. Join your fellow attendees, presenters and instructors for our kick-off event. It's a great way to meet up with old friends and make some new ones. There will be good company and good conversations - all that's missing is you.

### **POSTER SESSION • Tuesday, 4:25pm**

Authors will be available at their posters to answer questions and discuss their work during the Poster Session 4:25pm – 6:00pm, Tuesday. Posters (without authors) will be on display from Tuesday, 6:00pm until Thursday, 12:00pm

### **CONFERENCE BANQUET • Tuesday, 7:00pm**

In addition to a wonderful dinner and good conversation, **Dr. Rakesh Kumar** will speak on "Fabless Semiconductors...enabling a wealth of Opportunities"

There are over 1300 fabless Integrated Circuit companies worldwide, and over 20% of the worldwide semiconductor revenue now comes from fabless companies. And, there are two fabless companies among the Top 10 semiconductor companies. This talk will provide perspectives on the creation and management of successful entrepreneurship opportunities using the fabless business model.

Dr. Rakesh Kumar is President of TCX Technology Connexions, a services company which provides management, business and technical 'bridging the gaps' consulting in advanced semiconductor technology, and virtual operations areas. The TCX client list includes many emerging companies as well as some top 10 semiconductor companies. During 37 years in the semiconductor industry Dr. Kumar has held various technical and executive positions. He was VP & GM of the worldwide Silicon Technology Services business unit at Cadence Design Systems and Tality. At Unisys and Motorola he made technical and management contributions.

Dr. Kumar has authored the book "Fabless Semiconductor Implementation", published by McGraw Hill in 2008. Dr. Kumar is a Fellow of the IEEE and the President

of the IEEE Solid-State Circuits Society in 2012-13. Dr. Kumar is a Distinguished Lecturer of the IEEE Electron Devices and Solid-State Circuits Societies.

### **COOKOUT • Wednesday, 6:30pm**

Our conference would not be complete without our cookout! Combining great food, pleasant company and beautiful sunsets is all part of what makes our conference so special. The cookout is another great way to network and meet your fellow attendees. Relax and enjoy yourself and prepare for the Evening Panel Discussion which will follow.

### **EVENING PANEL • Wednesday, 8:00pm**

The topic for the Evening Panel is "FinFETs." This year's rump session focuses on long-term and most promising solution to CMOS scaling for the remaining few major nodes and possible flavors of each node thereof. FinFET is no longer a long-term research technology, albeit its first adoption being on bulk substrate rather than the founding substrate, SOI. Various FinFET topics such as scaling, applications, process, and substrate will be discussed by world-renowned experts. Lively discourse with the audience is expected as always.

### **LATE NEWS • Thursday, 3:35pm**

Submissions for the Late News Session will be accepted until August 29, 2011. Presentation of selected late papers will be on Thursday afternoon. Late News papers are not eligible for either the Best Paper Award or the Best Student Award. Additional information on Late Paper Submissions can be found on our website.

### **BEST OF CONFERENCE AWARDS**

We are pleased to present our two annual awards, the Best Paper Award and the Best Student Paper. The Best Paper Award recognizes the best paper of the conference as selected by our committee. The committee is also responsible for selecting and awarding the Best Student Paper. This paper is considered by the committee to be the top paper authored and presented by a student. Both of these honors are awarded at the close of the conference.

## AREA AND ACTIVITIES

### LOCATION

Home to Arizona State University, Tempe contains all the energy that you would expect from a college town and the attractions that you'd expect in the perfect vacation destination. Tempe is wonderfully situated to experience the beauty of the **Sonoran Desert**, with **Papago Park** to the north and **South Mountain Park** to the south. Tempe is part of the greater Phoenix area so you are within minutes of all that Phoenix and Scottsdale have to offer as well.

Some interesting and fun spots  
within an easy drive are:

- **The Phoenix Zoo** - Voted one of the Nation's top zoos for kids is just a mere 7 minutes away
- **Desert Botanical Gardens** - This professionally designed garden contains over 50,000 plant displays in beautiful outdoor exhibits.
- **Arizona Mills Outlet Mall** - A nice mix of traditional retail stores, value retail stores and entertainment venues.
- **Frank Lloyd Wright's Taliesin West** - Home of the Frank Lloyd Wright Foundation, Taliesin West began construction in 1937 and served as Wright's personal home in the winters. Tours are available, but you will need to call for the fall schedule.

For more information on Tempe and the Greater Phoenix area try the following links:

**Tempe Arizona Tourism Office**

**Scottsdale Visitors Bureau**

**Phoenix Visitors Bureau**

### WEATHER

Tempe enjoys sunny skies all year round and October is no exception. While you might be used to a cooler climates in October, Tempe boasts an average daily temperature of 87f / 29c. Business casual and sportswear are ideal for Tempe's daytime temperatures. You'll rarely need a topcoat and it is rarer still to see any rainfall. However, evenings can be cooler in a desert climate and Tempe is no exception. Expect temperatures to drop to around 56f / 13c after dark. So be sure to bring a jacket or a sweater.

### WEDNESDAY AFTERNOON

If you do not plan to attend the optional Fundamentals Class your Wednesday afternoon is free time. Being located in the heart of Downtown Tempe, you can easily stroll more than 100 shops, restaurants and galleries in the famed Mill Avenue District. Located nearby are Tempe Town Lake and the 2,000 acre Papago Park. Both offer a wide variety of outdoor activities. You can also just relax and enjoy a meal at The Mission Grille or any number of nearby restaurants. Then again, you can just simply enjoy the sun while enjoying the rooftop pool. Your options are endless!

## **AIRPORT AND TRANSPORTATION**

### **AIRPORT**

National and international air service for the region is provided through Phoenix Sky Harbor International Airport. The airport offers easy connection or direct flights to more than 85 domestic locations and 19 international locations. For more information see [Phoenix Sky Harbor International Airport](#)

### **RENTAL CARS**

The Phoenix Sky Harbor International Airport offers representation from all the major car rental companies. For a complete listing and contact information please see [Rental Cars](#).

### **PARKING**

Both valet and self parking are complimentary at the Tempe Mission Palms. There are limited self parking spaces available. Though there is no fee for parking, please bear in mind that Tempe Mission Palms bellmen work only for gratuities.

### **SHUTTLE SERVICE**

The Tempe Mission Palms offers a free shuttle service to and from Phoenix Sky Harbor International Airport between 5:30am and 10:30pm only.

Upon your arrival, you should proceed to the baggage claim area for your flight. Each terminal has a courtesy phone bank in the baggage claim area where you can place a call to the hotel by dialing #31 or you may dial the hotel directly (480) 894-1400. The hotel operator will ask which terminal you are in and direct you to the blue diamond sign. Tempe Mission Palms vans are white and have the hotel logo on them.

If you arrive outside of hotel shuttle hours, a taxi might be your best option. A ride from the airport to the hotel should cost between \$19 and \$30. Taxi terminal access is as follows: Terminal 2: North curbside, Terminal 3: North curbside, Terminal 4: Level 1, North curbside.

## CONFERENCE HOTEL

### Tempe Mission Palms Hotel and Conference Center

60 East Fifth Street, Tempe, Arizona 85281 • (480) 894-1400 • [www.missionpalms.com](http://www.missionpalms.com)

**Tempe Mission Palms Hotel and Conference Center** is an oasis in the heart of historic downtown Tempe, where you can relax in Mission-style comfort amid fireside seating areas and gentle fountains. Situated in downtown Tempe near Arizona State University (ASU), you are conveniently located just 10 minutes from **Phoenix Sky Harbor International Airport** and all major highways in and around the Phoenix and Scottsdale area.

The hotel is also located within walking distance to downtown Tempe's shopping, dining and entertainment district. You are only steps from the **Mill Avenue's** more than 170 shops, galleries, restaurants and popular Tempe entertainment venues.

Your room is designed to reflect the sprawling rose-colored deserts of the surrounding areas to help you relax at the end of the day. Featuring a variety of comfortable amenities and plush furnishings, the rooms are a residential style and provide views of Phoenix and the Valley of the Sun.

Tempe Mission Palms in-house Mission Grille serves traditional American and international cuisine. Diners can relax in the restaurant's elegant atmosphere and savor from a selection of artfully prepared dishes. The Mission Grille's regional cuisine gives their guests a taste of the special Southwestern fare iconic of the area, while Harry's Lounge is the meeting spot for enjoying cocktails and beers with friends and colleagues.

A spectacular rooftop swimming pool, two whirlpool spas, a fully equipped fitness center, and lighted tennis courts fill out the list of upscale amenities you can look forward to during your stay.

Tempe Mission Palms Business Center is equipped with the latest in computer technology, and offers a wide variety of services to accommodate your business and personal needs. For more information see **Tempe Mission Palms Business Center**.

#### HOW TO MAKE A RESERVATION

##### • VIA INTERNET

A dedicated web page has been created for conference attendees to book their sleeping rooms. Attendees are able to make, modify and cancel hotel reservations online.

**Tempe Mission Palms Reservations**

• **VIA TELEPHONE** +1 866 748 9146 - tell them you will be attending the IEEE International SOI Conference.

**HOTEL RATES** • The Tempe Mission Palms Hotel is pleased to offer the special, discounted rate of \$159 plus hospitality fee and tax (+\$10.95 +15.27%) single/double occupancy for conference attendees. This rate is good from Wednesday, September 28th through Sunday, October 9th. A major credit card or deposit is needed when you make a reservation to guarantee your room.

Please make sure to reserve your room by September 9, 2011 to ensure room availability. If you have a problem making a reservation, please contact the Conference Manager for assistance.

[manager@soiconference.org](mailto:manager@soiconference.org).

**HOSPITALITY FEE** • The Hospitality Fee of \$10.95 allows the hotel to provide a number of services. Airport transportation, wireless high speed internet access in your guest room, as well as local and toll-free telephone calls and incoming fax service, these are just a few of the amenities the fee covers.

**CHECK-IN/OUT TIMES** • Check-in time is 3:00pm and check-out time is 12:00pm.

**EXTRA PERSON IN ROOM** • A charge of \$10 per person will be added to the room rate for more than two adults in a room. Children 17 years and under may share the same room with parents at no additional charge.

## **CONFERENCE REGISTRATION**

### **ON-SITE CONFERENCE REGISTRATION SCHEDULE**

Sunday, October 2, 2011 .....	6:00pm – 8:00pm
Monday, October 3, 2011 .....	7:00am – 5:00pm
Tuesday, October 4, 2011 .....	7:00am – 5:00pm
Wednesday, October 5, 2011 .....	7:00am – 12:00pm
Thursday, October 6, 2011 .....	7:00am – 12:00pm

### **HOW TO REGISTER FOR THE CONFERENCE**

Complete the enclosed registration form. Please fill in all information completely.

Mail or fax your registration form and payment no later than September 23, 2011 to:

**IEEE International SOI Conference  
6930 De Celis Place, #36, Van Nuys, CA 91406  
or fax to: 818.855.8392**

Telephone registration is not available.

Please remember to include payment with your mailed or faxed form as only forms accompanied by payment will be accepted. There are no exceptions. You may pay for your registration with either check or credit card.

Do **not** send your hotel reservation form to the above address; you must send the hotel reservation form to the hotel.

### **CANCELLATIONS**

Cancellation requests must be made in writing to the conference manager. Refund requests received by September 23, 2011 will receive a refund of registration fees less a \$50 processing fee. Requests received after September 23, 2011 will be considered by the committee. All refunds will be processed after the conference.

### **TO PAY BY CREDIT CARD**

Complete the registration form including the CREDIT CARD INFORMATION section and mail it to:

**IEEE International SOI Conference  
6930 De Celis Place, #36, Van Nuys, CA 91406  
or fax to: 818.855.8392**

Please be sure that the credit card information is complete, legible, and includes your signature.

### **TO PAY BY CHECK**

Complete the registration form and mail it with your check to:

**IEEE International SOI Conference  
6930 De Celis Place, #36, Van Nuys, CA 91406  
or fax to: 818.855.8392**

Please make the check payable to 2011 IEEE SOI Conference. All checks **must** be drawn on a US bank and in US funds only. Registration forms received without payment will not be honored.

### **BANK - WIRE TRANSFERS**

While payment may be made via bank transfer (by wiring funds), it is discouraged and there is an additional \$25.00 fee per transfer to cover handling costs. If a bank transfer is necessary, please contact the Conference Manager at [manager@soiconference.org](mailto:manager@soiconference.org) for further instructions and the appropriate account numbers.

